

1 Introduction

This document describes the estimated product lifetimes for the i.MX RT1010 applications processors based on the criteria used in the qualification process.

The product lifetimes described here are estimates and do not represent a guaranteed lifetime of the processor.

The i.MX RT series consist of an extensive number of processors that deliver a wide range of processing and multimedia capabilities across various qualification levels.

This document guides on how to interpret different i.MX RT1010 qualification levels in terms of the target operating frequency of the device, the maximum supported junction temperature (T_j) of the processor, and how this relates to the lifetime of the device.

Each qualification level supported, commercial and industrial, defines a number of Power-on Hours (PoH) available to the processor under a given set of conditions, such as:

- The target frequency for the application, commercial and industrial.
 - The target frequency is determined by the input voltage to the processor's core complex ($V_{DD_SOC_IN}$).
 - The use of the DCDC-enabled or DCDC-bypass modes.
 - When using the DCDC-bypass mode, the target voltage should not be set to the minimum specified in the datasheet. All power management ICs have allowable tolerances. The target voltage must be set higher than the minimum specified voltage to account for the tolerance of the PMIC. The tolerance assumed in the calculations in this document is ± 25 mV.
 - The DCDC-enabled mode uses the DCDC module to create a power supply for the core logic on the i.MX RT series. The DCDC module is well characterized and can be set to output the exact minimum specified voltage. Longer Power-on-Hours can be achieved using the DCDC-enabled mode.
- The percentage of active use compared to standby.
 - Active use means that the processor is running in an active performance mode.
 - For the commercial tiers, there are two performance modes available: 500 MHz and 400 MHz.
 - In the DSM mode, the datasheet defines lower operating conditions for $V_{DD_SOC_IN}$, reducing the power consumption and junction temperature. In this mode, the voltage and temperature are set low enough so that the effect on the lifetime calculations is negligible and treated as if the device was powered off.
- The junction temperature (T_j) of the processor.
 - The maximum junction temperature of the device is different for each tier of the product. For example, 95 °C for commercial and 105 °C for industrial. This maximum temperature is guaranteed by the final test.

Ensure that your device is appropriately thermally managed and the maximum junction temperature is not exceeded.

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NOTE

All data provided within this document are estimates for the PoH that are based on extensive qualification experience and testing with the i.MX RT series. These statistically derived estimates must not be viewed as a limit on an individual device's lifetime, nor construed as a guarantee by NXP as to the actual lifetime of the device. The sales and warranty terms and conditions still apply.

2 Device qualification level and available PoH

2.1 Commercial qualification

[Table 1](#) provides the number of PoH for the typical use conditions for the commercial device.

Table 1. Commercial qualification lifetime estimates

—	Arm [®] core speed (MHz)	Power-on Hours [PoH] (Hrs)	Arm core operating voltage (V)	Junction temperature [Tj] (°C)
Case C1: DCDC Enabled	500	28,098	1.25	95
Case C2: DCDC Enabled	400	76,379	1.15	95
Case C3: DCDC Bypassed	500	21,883	1.275	95
Case C4: DCDC Bypassed	400	59,484	1.175	95

[Figure 1](#) and [Figure 2](#) establish the guidelines for estimating the PoH as a function of CPU frequency and junction temperature. The PoH can be read directly off the charts below to determine the necessary trade-offs for the CPU frequency and junction temperature to increase the estimated PoH of the device.

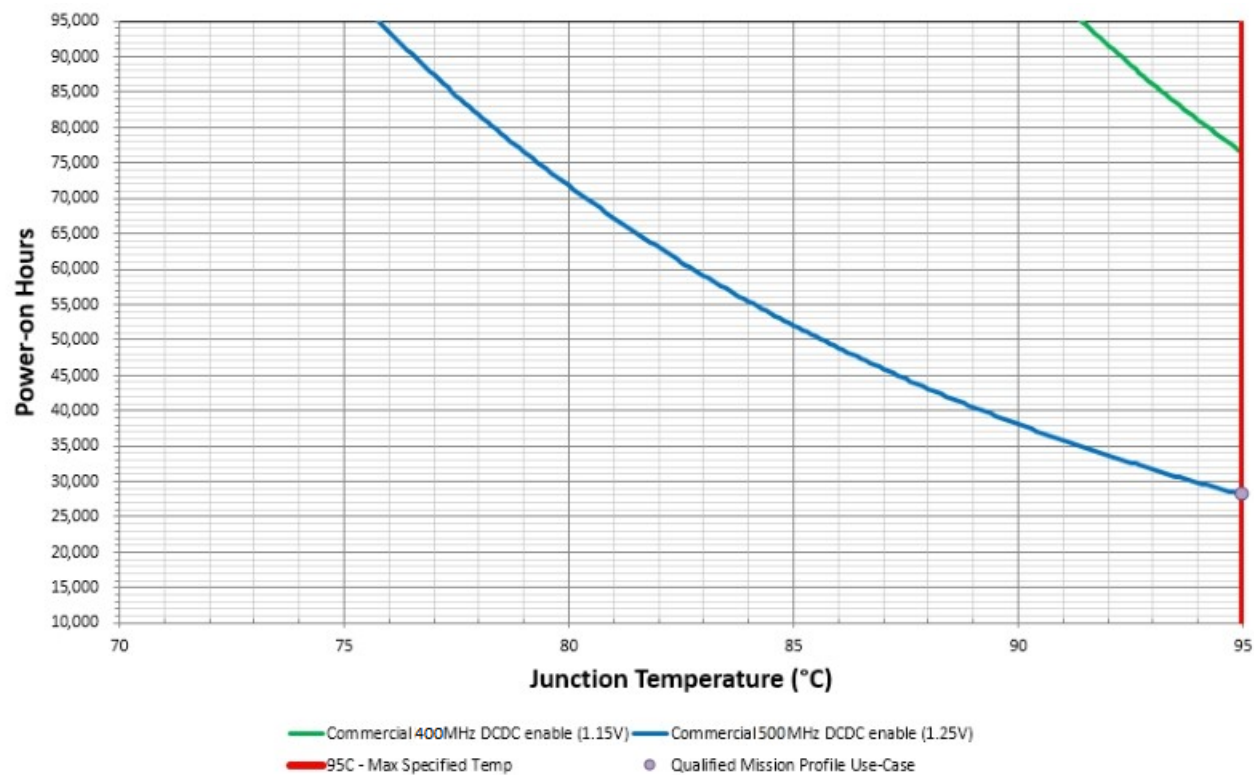
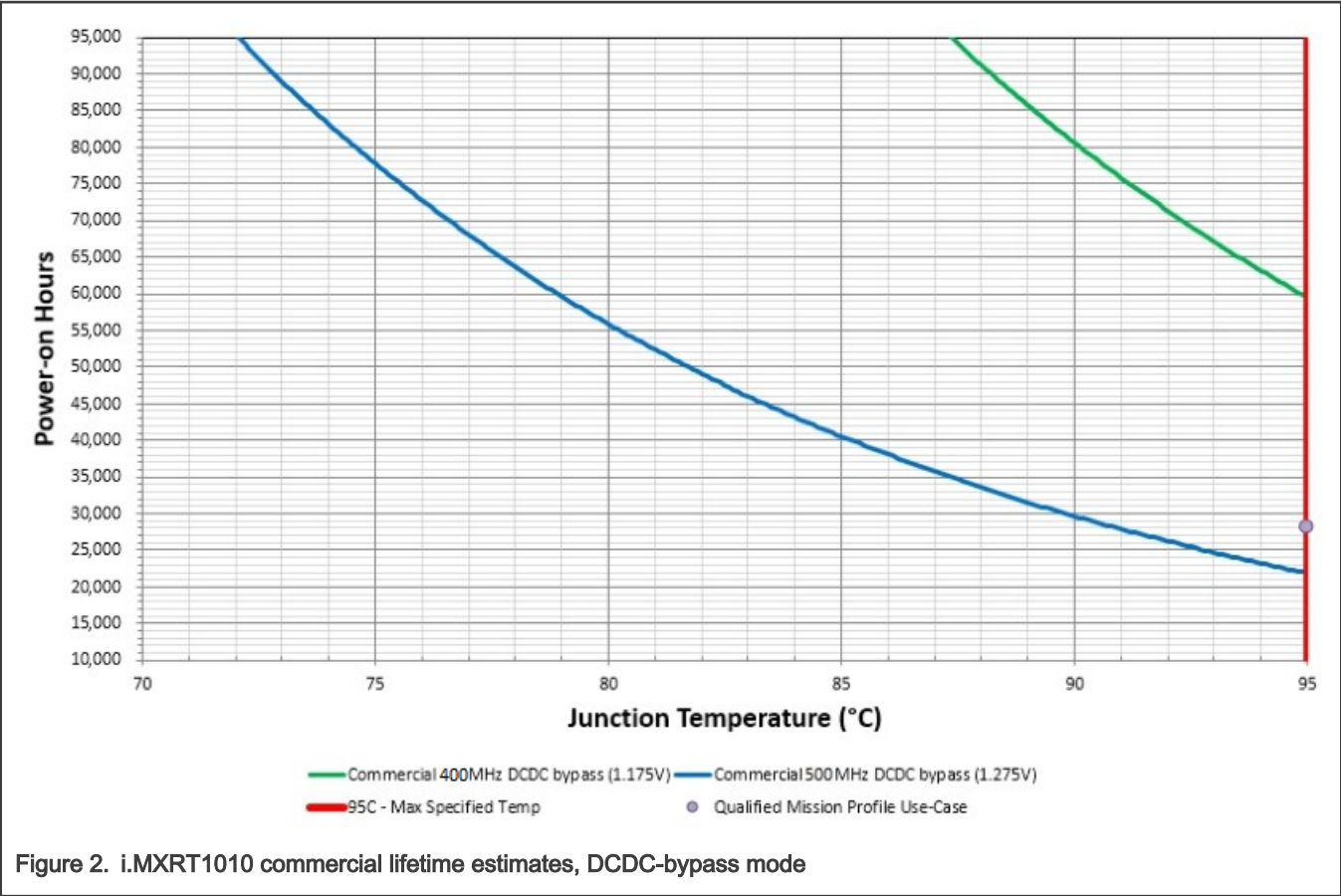


Figure 1. i.MXRT1010 commercial lifetime estimates, DCDC-enabled mode



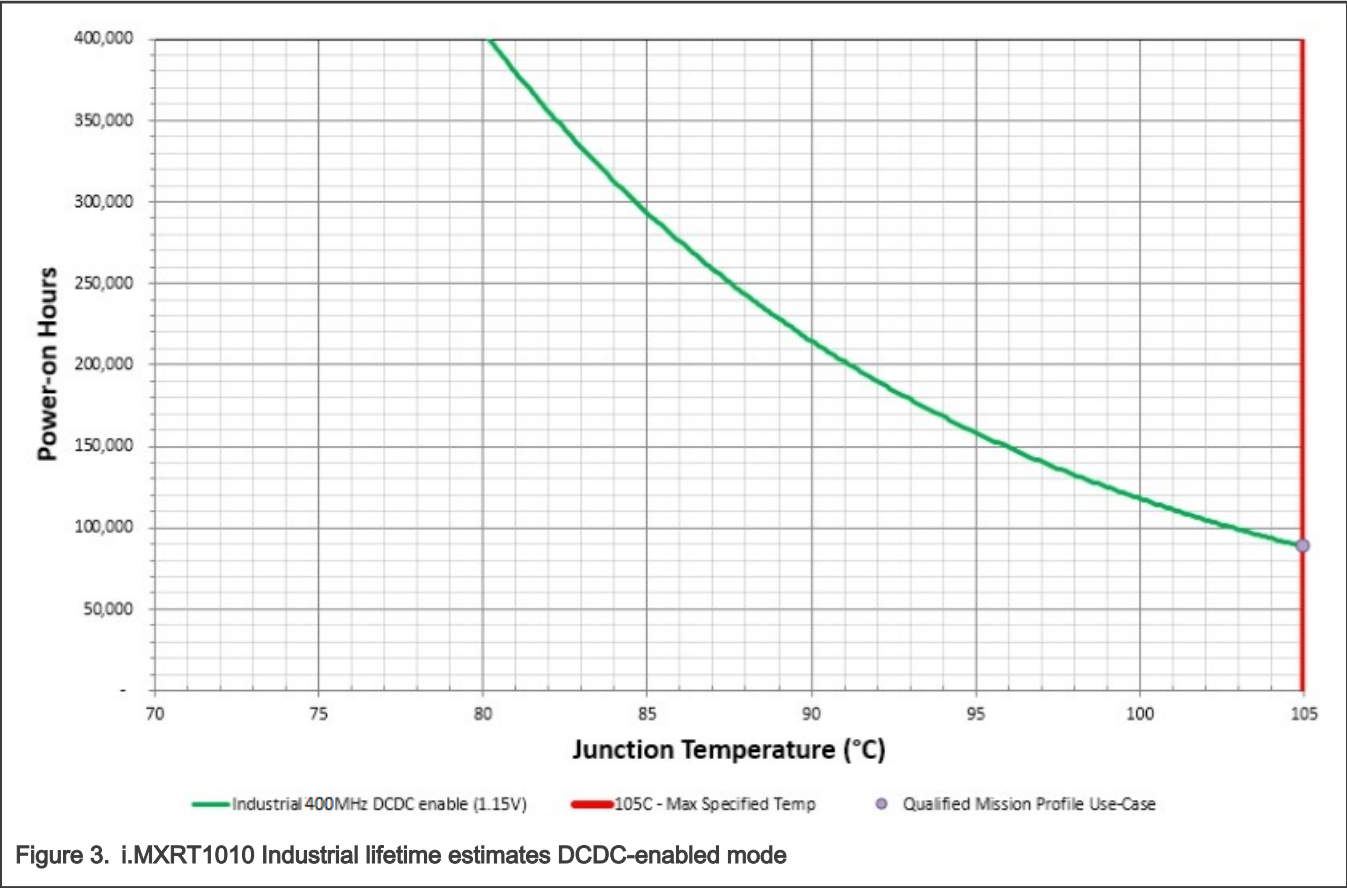
2.2 Industrial qualification

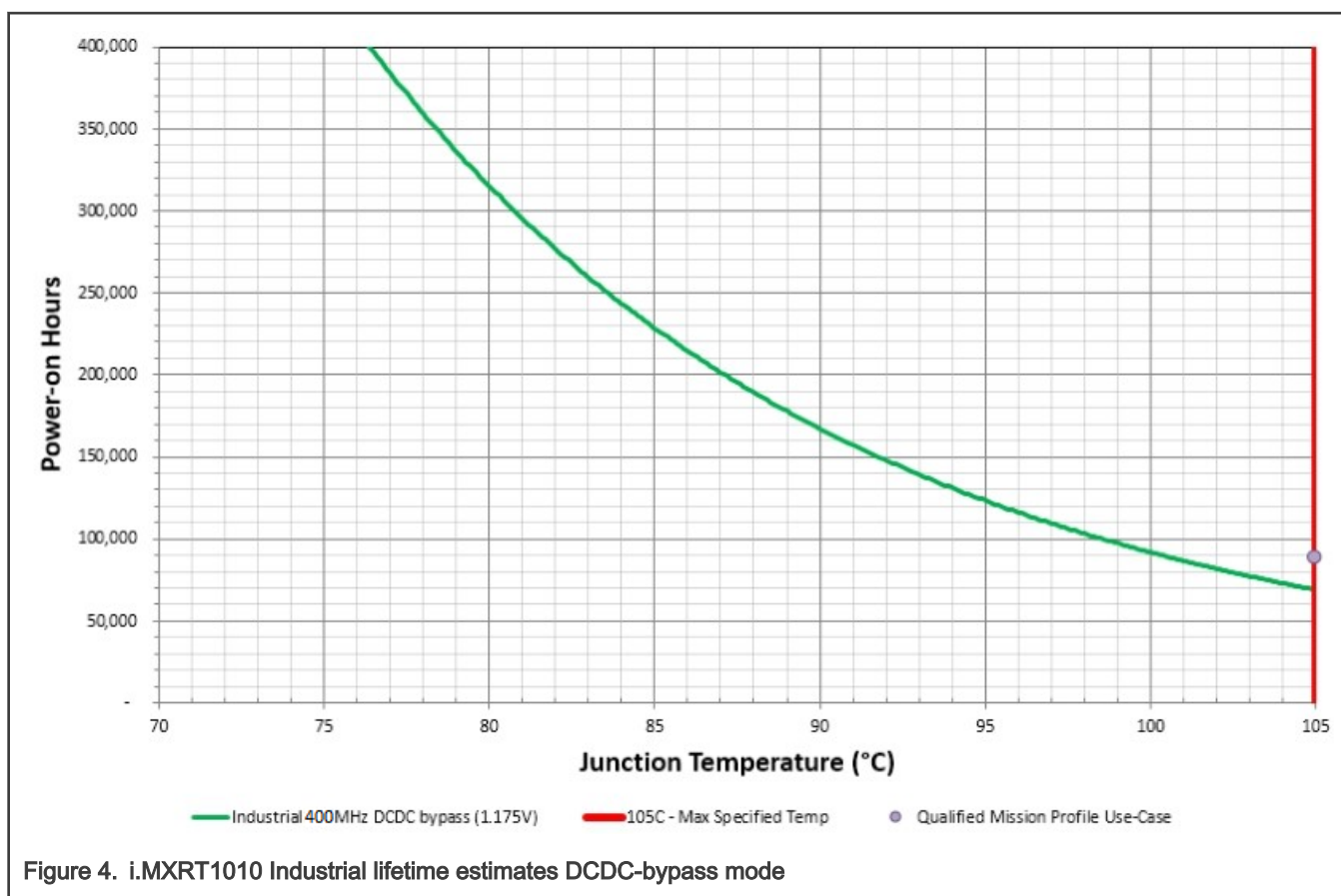
Table 2 provides the number of PoH for the typical use conditions for the industrial device.

Table 2. Industrial qualification lifetime estimates

—	Arm core speed (MHz)	Power-on Hours [PoH] (Hrs)	Arm core operating voltage (V)	Junction temperature [Tj] (°C)
Case I1: DCDC enabled	400	88,407	1.15	105
Case I2: DCDC bypassed	400	68,851	1.175	105

Figure 3 and Figure 4 establish the guidelines for estimating the PoH as a function of CPU frequency and junction temperature. The PoH can be read directly off the charts below to determine the necessary trade-offs for the CPU frequency and junction temperature to increase the estimated PoH of the device.



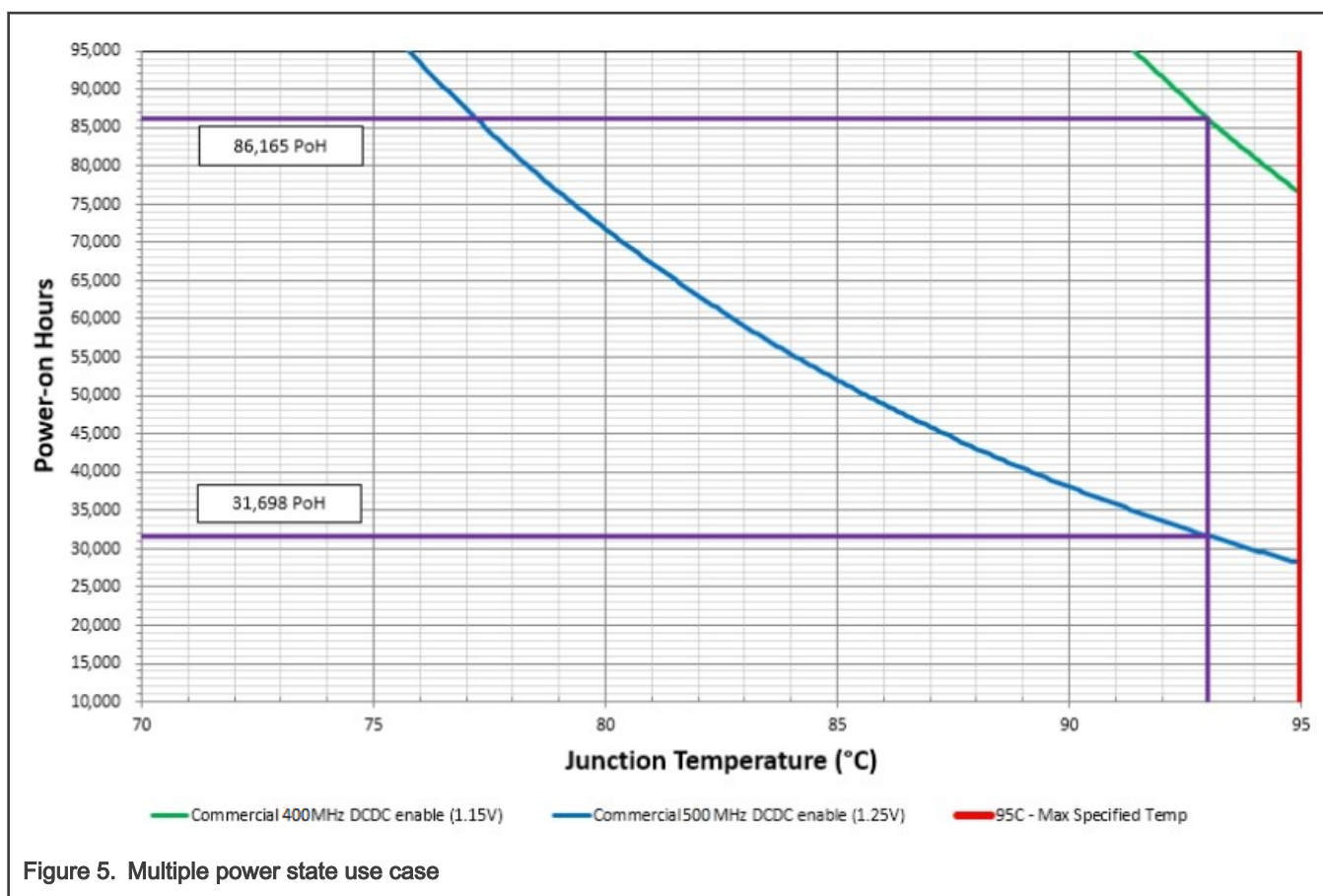


3 Combining use cases

In some applications, a constant operating use case cannot deliver the target PoH. In this case, it is better to use multiple operating conditions. This method provides some of the lifetime benefits of running at a lower performance use case, while keeping the ability of the system to use the highest performance state dictated by the application's demands.

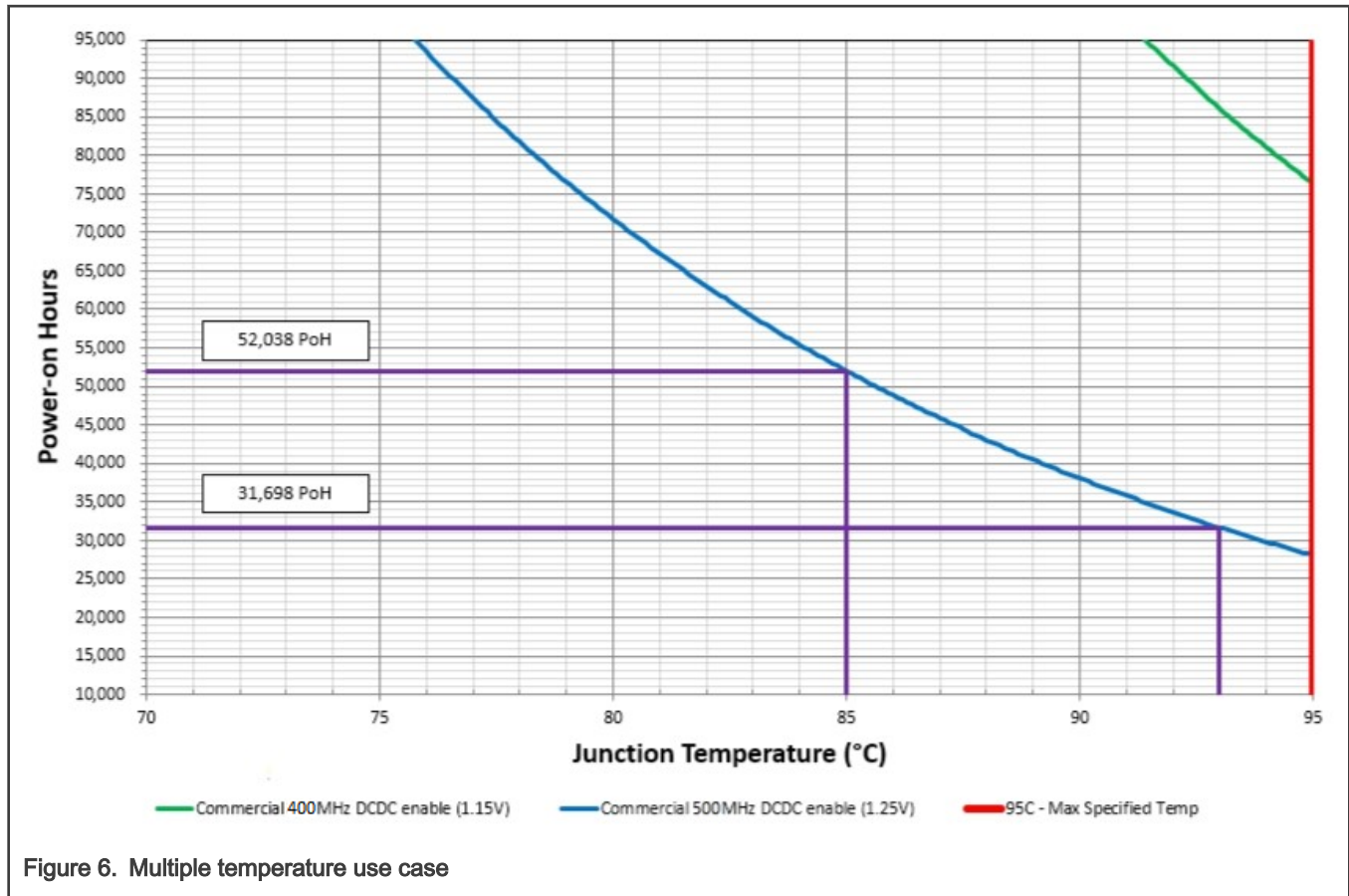
3.1 Scenario 1: Switching between two power states with different voltages

In this scenario, the system is using the 500 MHz full-power state, and the 400 MHz reduced-power state. For these calculations, it is assumed that the temperature stays constant in either mode. If the system spends 50 % of its power-on-time at 500 MHz and 50 % of its power-on-time at 400 MHz, the two POH, as shown in [Figure 5](#), can be combined with using those percentages: $31,698 \times 0.5 + 86,165 \times 0.5 = 58,931$ PoH.



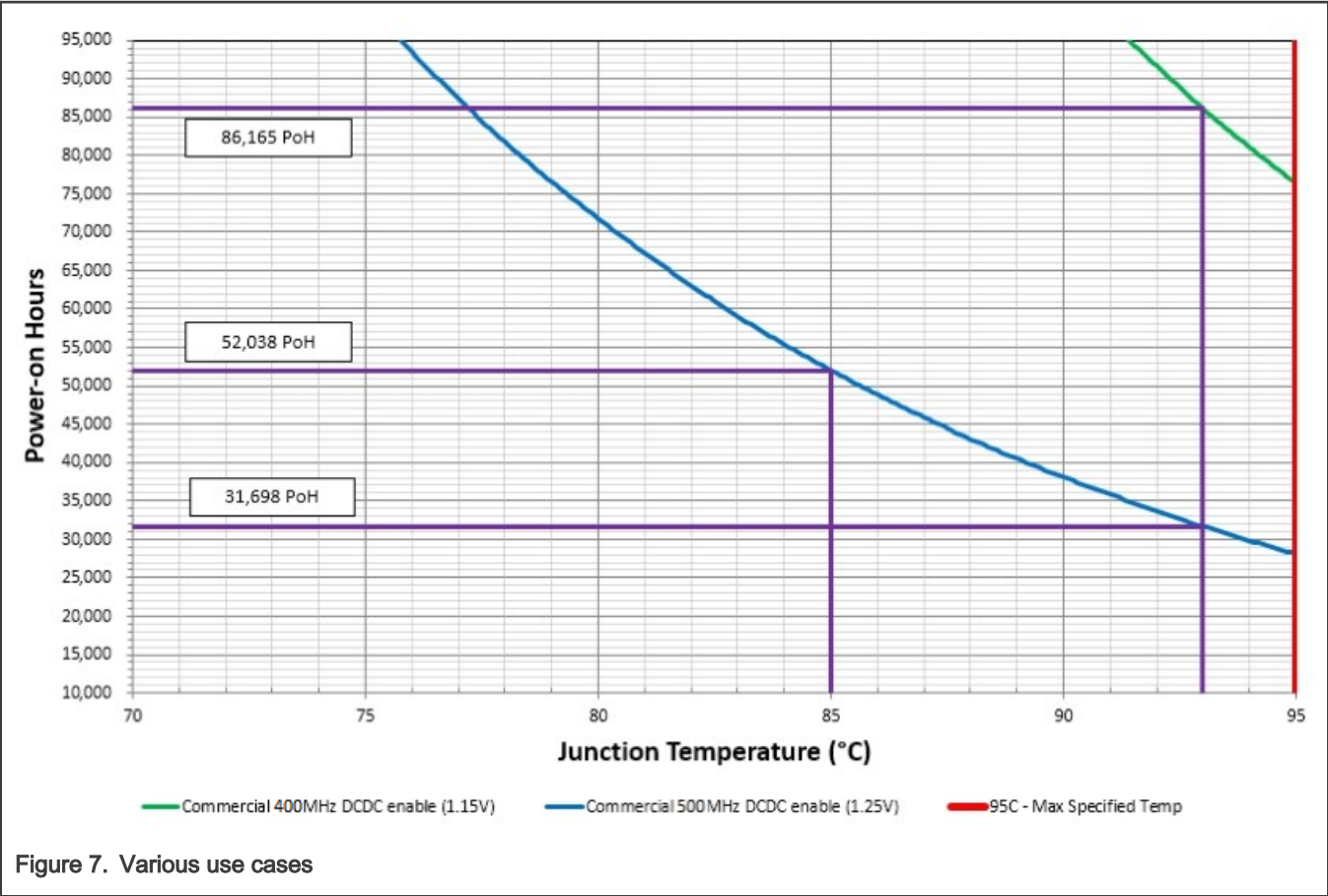
3.2 Scenario 2: Switching between two power states with different temperatures

This scenario assumes that the system can achieve a drop-in temperature by throttling back the performance while still maintaining a constant voltage. This temperature change can be achieved by changing the frequency or by simply scaling back the load on the Arm cores (or processing units). This use case is particularly useful for users who need to take advantage of the full commercial temperature range of the i.MX RT MCUs. In this scenario, the system spends 30 % of its PoH at 93 °C and 70 % of its power-on hours at 85 °C, as shown in Figure 6. The two PoHs can be combined as follows: $31,698 \times 0.3 + 52,038 \times 0.7 = 45,932$ PoH.



3.3 Scenario 3: Using three or more power states

This scenario shows how to extend this strategy to more than two power states. While this example has only three power states, there is no limit to the actual number of the power states that can be combined. The power states that are being used in this scenario are 400 MHz (at 93 °C) and 500 MHz (at 85 °C and 93 °C). Each state is used one third of the time. These power states can be combined as follows: $86,165 \times 0.34 + 52,038 \times 0.33 + 31,298 \times 0.33 = 56,796$ PoH.



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For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10/2020

Document identifier: AN13025

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