AN13031

Recommendations for SD Connections to 1.8 V SDHC Interfaces

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by: NXP Semiconductors

Contents

1 Introduction

The enhanced Security Digital Host Controller (eSDHC) in the LX216x and LS208xA conform to the SD Host Controller Standard Specification version 3.0. They are compatible with the SD Memory Card Specification version 3.01 (SDXC SDHC, SD cards), and the SDIO Card Specification version 3.0. And they are also compatible with the JESD84-B51 (eMMC/MMC cards) and JESD84-B45 respectively. The eSDHC interface can be used to get the Reset Configuration Word (RCW), Pre-Boot Initialization (PBI), booting images from an SD card or from an eMMC. eSDHC can also be used as an interface of storage. There is no issue for the eSDHC interface when it works with an 1.8-volt eMMC as it is an 1.8 V interface on both parts. However, a voltage translator must be used if it interfaces with any type of SD card, such as SDXC, SDHC, and SD cards. It is the requirement of the SD Specification Part 1 Physical Layer Specification 3.0 that the starting voltage is 3.3 V for any type of SD card.

This application note gives an example design when the eSDHC is interfaced with an SD card. Schematics for connecting to a voltage translator will be discussed.

2 Recommended schematics

Several voltage translators on the market can be used for the eSDHC interface. NXP recommends to use NVT4857UK as it supports High Speed (HS) and UHS-I speeds. It supports up to 208 MHz clock rate. Figure 1 shows the recommended circuit when SDR speeds are needed.

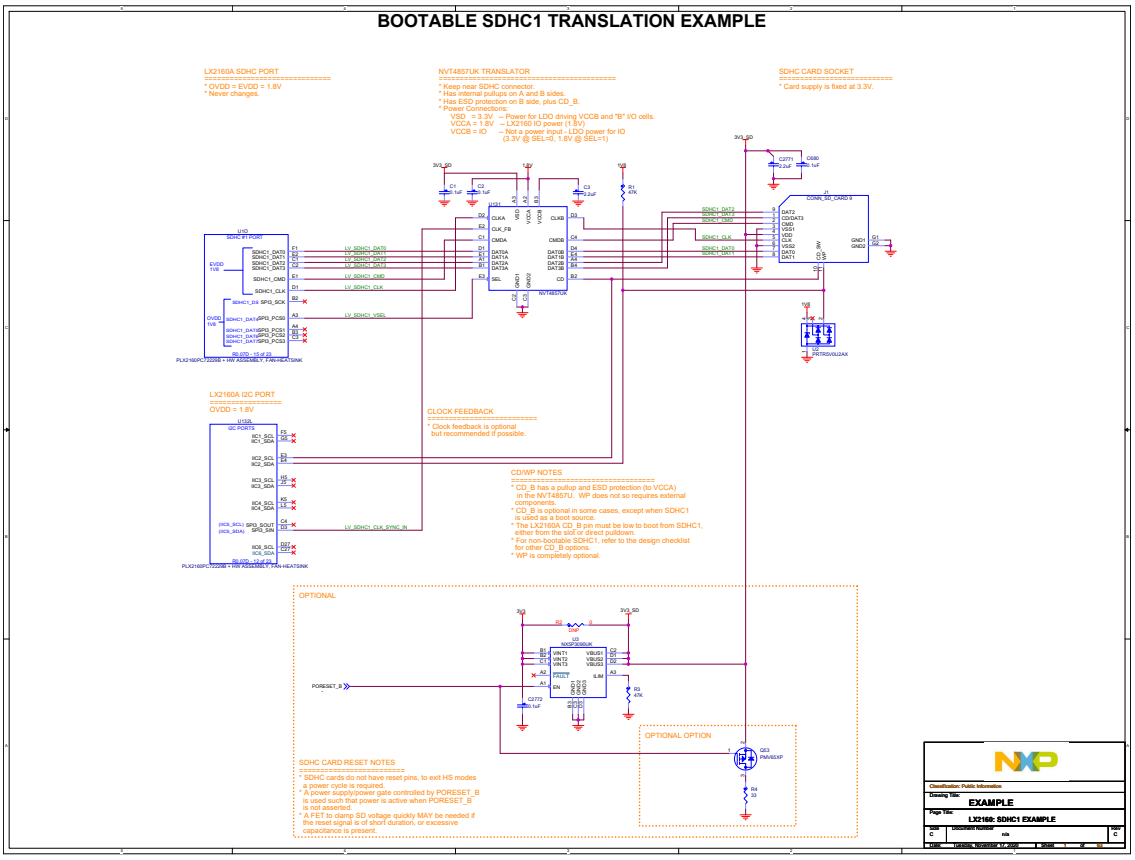

Figure 1. Recommended voltage translator schematics

The SD card signaling voltage is 1.8 V when it is configured to run at an SDR speed. Based on the SD specification, **once signal voltage is swithced to 1.8 V, the card continues 1.8 V signalling regardless of CMD0. Power cycle reset the signal voltage to 3.3 V**. Therefore, a period of power-off is needed for the SD after a reset.

The power-off design can be avoided if HS mode can meet system requirements. Figure 2 shows the recommended circuit when only HS speed is needed. In this case, no power-off SD card circuit is needed as the signaling voltage runs at 3.3 V.

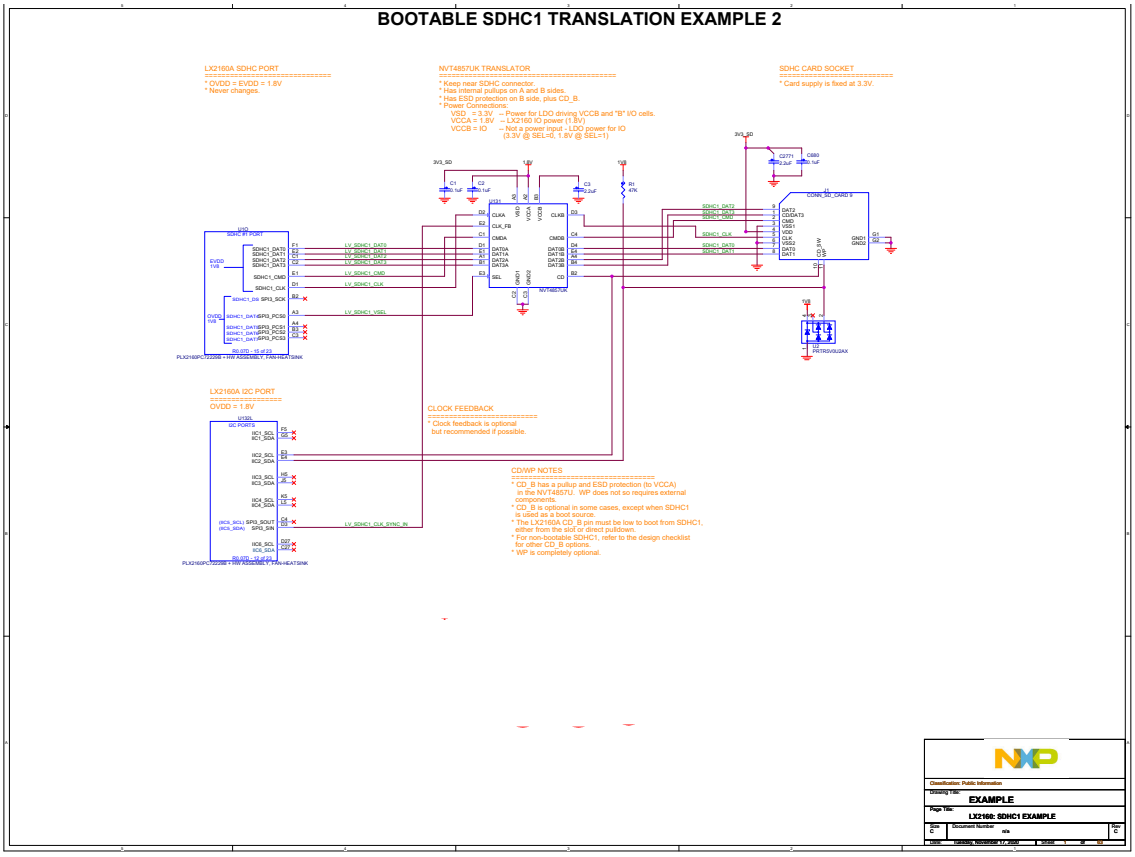

Figure 2. Recommended voltage translator schematics without resetting SD card circuit

As you can see from Figure 1 and Figure 2, the difference between these two designs is the power-off circuit. The design of this circuit should meet the SD specification requirement of keeping power level less than 0.5 V and more than 1 ms.

3 AC timing considerations

eSDHC interface on LX2160xA supports both SDR50 and DDR50 modes. This section gives the AC timing specifications for SDR50 and DDR50 based on the recommended NVT4857UK part.

Table 1 provides the eSDHC AC timing specifications for SDR50 mode.

Table 1. eSDHC SDR50 mode AC timing specifications with a voltage translator

Parameter	Symbol[1]	Min.	Max.	Unit	Notes
SDHC_CLK clock frequency	f_{SHSCK}	0.0	100.0	MHz	—
SDHC_CLK rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	2.0	ns	2
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN),	$t_{SHSIVKH}$	1.9	—	ns	2, 4, 5

Table continues on the next page...

Table 1. eSDHC SDR50 mode AC timing specifications with a voltage translator (continued)

Parameter	Symbol[1]	Min.	Max.	Unit	Notes
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHSIXKH}$	0.7	—	ns	2, 4, 5
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	1.6	—	ns	2, 5, 6
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	—	5.7	ns	2, 5, 6

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF.
3. Sampled and not 100% tested
4. See Figure 3
5. The voltage translator parameters are based on:
   - Channel-to-channel skew is min -0.5 ns, max +0.5 ns.
   - CLK_Feedback to DAT/CMD delay is min -0.5 ns, max +0.5 ns.
6. See Figure 4

Figure 3 provides the eSDHC input AC timing diagram for SDR50 mode.

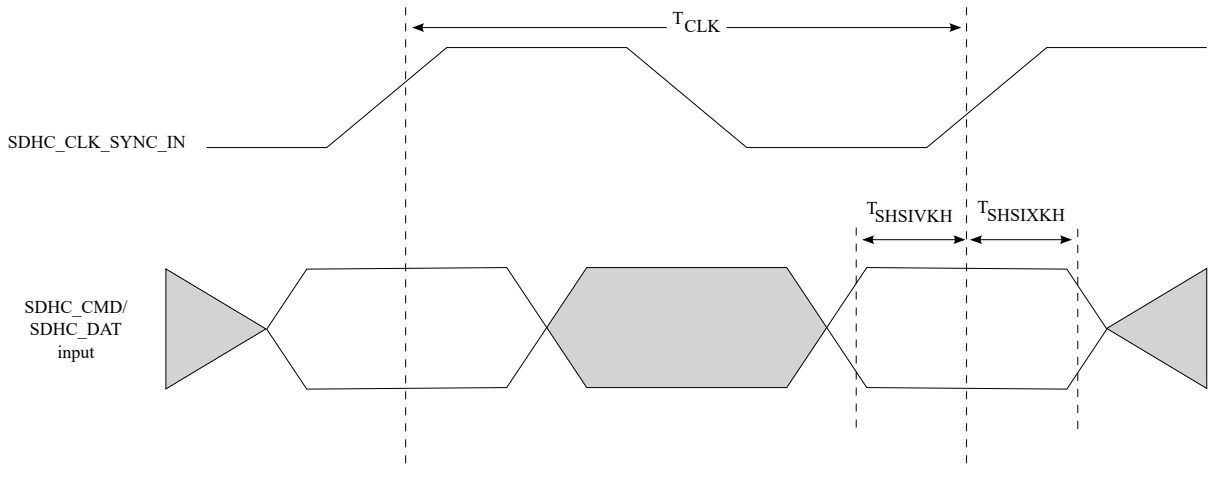

Figure 3. eSDHC SDR50 mode input AC timing diagram

Figure 4 provides the eSDHC output timing diagram for SDR50 mode.

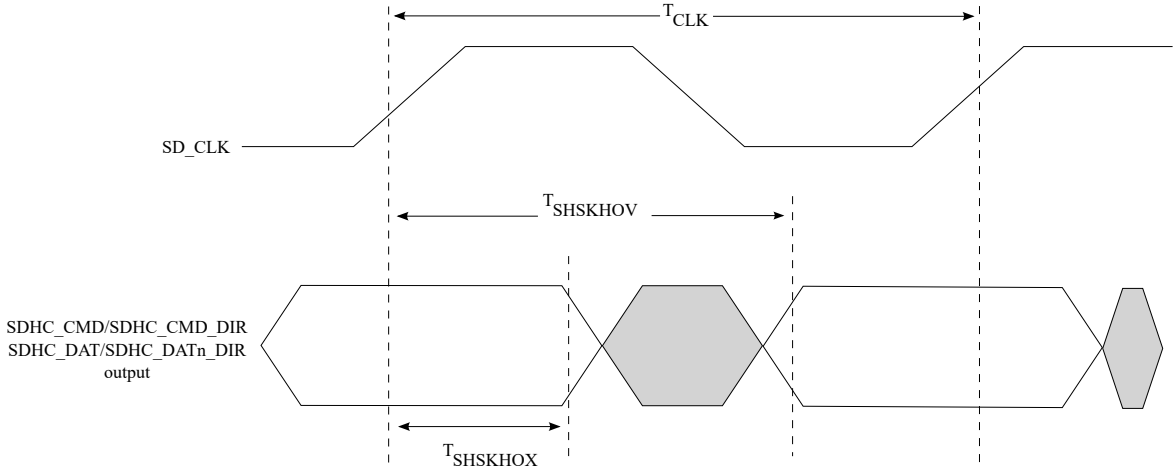

Figure 4. eSDHC SDR50 mode output timing diagram

Table 2 provides the eSDHC AC timing specifications for DDR50 mode with a voltage translator.

Table 2. SDHC AC timing specifications for DDR50 mode with a voltage translator

Parameter	Symbol[1]	Min.	Max.	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	0.0	50.0	MHz	2
SDHC_CLK rise and fall times	t_{SHCKR}/ t_{SHCKF}	—	4.0	ns	2, 3
SDHC_CLK duty cycle	t_{SHCK}	47.0	53.0	%	2, 4
Input setup times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIVKH}$	1.6	—	ns	2, 3, 5, 6
Input hold times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIXKH}$	0.7	—	ns	2, 3, 5, 6
Output hold time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOX}$	2.2	—	ns	2, 3, 6, 7
Output delay time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOV}$	—	5.6	ns	2, 3, 6, 7
Input setup times (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIVKH}$	4.8	—	ns	2, 3, 5, 6
Input hold times (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIXKH}$	0.7	—	ns	2, 3, 5, 6
Output hold time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOX}$	2.2	—	ns	2, 3, 6, 7
Output delay time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOV}$	—	12.6	ns	2, 3, 6, 7

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters

representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 25pF$ for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.
3. $C_{CARD} \leq 10$ pF, (1 card)
4. Sampled and not 100% tested
5. See **eSDHC DDR50/DDR mode input AC timing diagram** in *QorIQ LX2162A/LX2122A/LX2082A Data Sheet*.
6. The voltage translator parameters are based on:
   - Channel-to-channel skew is min -0.5 ns, max +0.5 ns.
   - CLK_Feedback to DAT/CMD delay is min -0.5 ns, max +0.5 ns.
7. See **eSDHC DDR50/DDR mode output AC timing diagram** in *QorIQ LX2162A/LX2122A/LX2082A Data Sheet*.

4 References

SD Specifications, Part 1, Physical Layer Specification Version 3.01

QorIQ LX216xA Data Sheet, where x can be either 0 or 2

QorIQ LS20xyA Data Sheet, where x can be either 8 or 4, y can be 0, 1, 4 or 8

QorIQ LS2088A Reference Manual

QorIQ LX2160A Reference Manual

QorIQ LX2162A Reference Manual

JESD84-B51, Embedded Multi-Media Card (eMMC) Electrical Standard (5.1)

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