AN13818

LPC86x Low-power and Wake-up Optimization

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Document Information

Information	Content
Keywords	LPC86x, low power
Abstract	This application note introduces how to optimize the power consumption and wake-up time with the low-power feature.

1 Introduction

The low-power feature is an important demand in most of consumer applications. To reduce the power consumption and wake-up time, set the chip into different power modes and turn off these unused modules or reduce the system clock. This application note introduces how to optimize the power consumption and wake-up time with the low-power feature.

2 LPC86x overview

The LPC86x is an Arm Cortex-M0+ based, low-cost 32-bit MCU operating at CPU frequencies of up to 60 MHz in LPC series. It supports up to 64 kB of flash memory and 8 kB of SRAM.

The peripheral complements of the LPC86x include a CRC engine, one I3C bus interface, one I2C bus interface, up to three USARTs, up to two SPI interfaces, one multirate timer, self-wake-up timer, two FlexTimers, one general-purpose 32-bit counter/timer, a DMA, one 12-bit ADC, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 54 general-purpose I/O pins.

Features relevant to power include:

- Reduced power modes and wake-up:
  - Integrated Power Management Unit (PMU) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep sleep mode and Power-down mode on activity on USART, SPI, I2C, and I3C peripherals.
- Timer-controlled self-wake-up from Deep power-down mode.
  - Power-On Reset (POR)
  - Brownout detect (BOD)
  - Single power supply 1.8 - 3.3 v

3 Power management

Figure 1 shows the four low-power modes. And in different power modes, the peripherals can be software configurable or power on/off automatic. When the low-power feature is used, only FRO or low-power oscillator can afford the system clock.

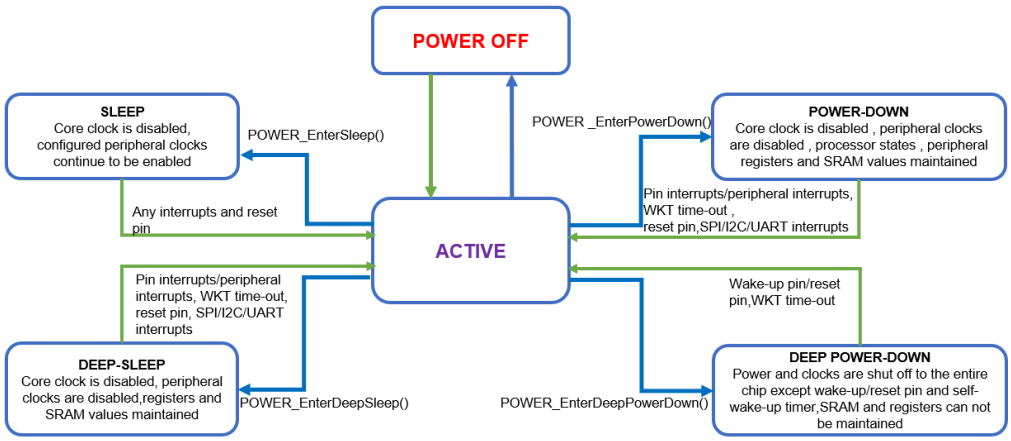

Figure 1. Power mode transition diagram

Note: *When the chip enters Deep sleep mode, Power-down mode, or Deep power-down mode, FRO provides the system clock and the FRO output (FRO divider) is disabled. The system can only set to FRO18M/FRO24/FRO30/FRO36M/FRO48M/FRO60M before entering the Deep sleep mode or Power-down mode.*

Table 1. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep sleep mode	Power-down mode	Deep power-down mode
FRO	Software configurable	ON	OFF	OFF
FRO output	Software configurable	OFF	OFF	OFF
Flash	Software configurable	ON	OFF	OFF
BOD	Software configurable	Software configurable	Software configurable	OFF
PLL	Software configurable	OFF	OFF	OFF
SysOsc	Software configurable	OFF	OFF	OFF
WDosc/WWDT	Software configurable	Software configurable	Software configurable	OFF
Digital peripherals	Software configurable	OFF	OFF	OFF
WKT/Low-power oscillator	Software configurable	Software configurable	Software configurable	Software configurable
ADC	Software configurable	OFF	OFF	OFF
Comparator	Software configurable	OFF	OFF	OFF

3.1 Power modes

There are five power modes on LPC86x listed as below, from highest to lowest:

1. Active mode:
   The part is in active mode when it is fully powered and operational after booting.
2. Sleep mode:
   This mode can only affect the Arm Cortex-M0+ core. Peripherals and memories are active.
3. Deep sleep mode and Power-down mode:
   - Deep sleep mode and Power-down mode cannot only affect the core. These two modes can also affect memories and peripherals.
   - In the Deep sleep mode, the peripherals receive no internal clocks. The flash is in standby mode. The SRAM memory and all peripheral registers as well as the processor maintain their internal states. The WWDT, WKT, and BOD can remain active to wake up the system on an interrupt.
   - In the Power-down mode, different from the Deep sleep mode, the flash memory is powered down.
4. Deep power-down mode:
   In the Deep power-down mode, the entire system is shut down. Only the general-purpose registers in the PMU register maintain internal states and the self-wake-up timer is not shut down. The WAKEUP pin or chip RESET can wake it up.

3.2 Wake-up process

Wake-up sources can wake up chip in different power modes, such as, peripherals interrupts, Self-wake-up timer, reset pin. Table 2 describes the wake-up sources for different power modes.

Table 2. Wake-up sources for power modes

Power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
	RESET pin PICO_5	Enable the reset function in the PINENABLE0 register via switch matrix.
Deep-sleep and Power-down	Pin interrupts	Enable pin interrupts in NVIC and STARTERP0 register via switch matrix
	BOD interrupts	• Enable interrupt in NVIC and STARTERP1 registers. • Enable interrupt in BODCTRL register. • BOD powered in PDSLEEPCFG register.
	BOD reset	• Enable interrupt in BODCTRL register. • BOD powered in PDSLEEPCFG register
	WWDT interrupts	• Enable interrupt in NVIC and STARTERP1 registers. • WWDT running. Enable WWDT in WWDT MOD register and feed. • Enable reset in WWDT MOD register. • WDOsc powered in PDSLEEPCFG register.
	WWDT reset	• WWDT running. • Enable reset in WWDT MOD register. • WDOsc powered in PDSLEEPCFG register.
	Self-wake-up Timer (WKT) time-out	• Enable interrupt in NVIC and STARTERP1 registers. • Enable ultra low-power oscillator in the DPDCTRL register in the PCON block. • Select low-power clock for WKT clock in the WKT CTRL register. • Start the WKT by writing a time-out value to the WKT COUNT register.
	Interrupt from USART/SPI/I2C peripheral	• Enable interrupt in NVIC and STARTERP1 registers. • Enable USART/SPI/I2C interrupts. • Provide an external clock signal to the peripheral. • Configure the USART in synchronous slave mode and I2C and SPI in slave mode.
	Interrupt from peripheral	• Enable interrupt in NVIC and STARTERP1 registers. • Switch FCLK clock source to the WDOsc.
	RESET pin PIO0-5	Enable the reset function in the PINENABLE0 register via switch matrix.
Deep power-down	WAKEUP pin PIO0-4	Enable the WAKEUP function in the DPDCTRL register in the PMU.
	RESET pin PIO0_5	Enable the reset function in the DPDCTRL register in the PMU to allow wake-up in the Deep power-down mode.
	WKT time-out	• Enable the ultra low-power oscillator in the DPDCTRL register in the PMU. • Enable the ultra low-power oscillator to keep running in deep power-down mode in the DPDCTRL register in the PMU. • Select low-power clock for WKT clock in the WKT CTRL register. • Start **WKT** by writing a time-out value to the WKT COUNT register.

4 Power configurations

The LPC86x supports a variety of power control features. In the active mode, when the chip is running, to optimize power and clocks to selected peripherals for power consumption, configure registers. In the four reduced power modes (sleep, deep-sleep, power-down, and deep power-down), to optimize the power consumption and to select the wake-up source, set the registers to different modes.

4.1 Active mode

In the active mode, clock the Arm Cortex-M0+ core, memories, and peripherals with the system clock or main clock.

The chip runs in active mode after reset. The default power configuration is determined by the reset values of the `PDRUNCFG` and `SYSAHBCLKCTRL` registers. The power configuration can be changed during the runtime.

4.2 Sleep mode

In sleep mode, the core clock stops and execute the instructions when a reset or interrupt occurs.

To configure power consumption in sleep mode, perform the same settings as in the active mode:

- The clock remains running.
- The system clock frequency remains the same as in the active mode, but the processor is not clocked.
- Analog and digital peripherals are selected as in the active mode.

4.3 Deep sleep mode

In the Deep sleep mode, the system clock remains, but it is not clocked to the processor. All analog blocks are powered down, except for the BOD circuit and the low-power oscillator, which can be selected or deselected during the Deep sleep mode in the `PDSLEEPCFG` register.

As shown in Figure 1, the Deep sleep mode powers off all the analog peripherals and eliminates all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

Power consumption in Deep sleep mode is determined by the deep-sleep power configuration setting in the `PDSLEEPCFG` register:

- The low-power oscillator can be left running in the Deep sleep mode if required for the WWDT.
- The BOD circuit can be left running in the Deep sleep mode if required by the application.

4.4 Power-down mode

In the Power-down mode, the system clock to the processor and analog blocks power configuration are same as the Deep sleep mode. If the low-power oscillator is selected. The main clock and therefore all peripheral clocks are disabled except for the clock to the watchdog timer. FRO and flash are powered down Compared to the Deep sleep mode, the power consumption decreases.

Peripheral configurations in the Power-down mode are same as the Deep sleep mode Compared to the Deep sleep mode, its wake-up time is longer.

Configure the power consumption the in the Power-down mode with the power configuration setting in the `PDSLEEPCFG` register, same as for the Deep sleep mode.

4.5 Deep power-down mode

As shown in Table 1, the Deep power-down mode has no configuration options. All clocks, the core, and all peripherals are powered down. Only the WAKEUP pin, RESET pin, and the self-wake-up timer are powered.

During the Deep power-down mode, the contents of the SRAM and registers are not retained except for a small amount of data which can be stored in the general-purpose registers of the PMU blocks.

5 Example to achieve typical data on data sheet

5.1 Hardware environment

- LPCXpresso860-MAX EVK
- Personal computer
- USB cable
- Digital multimeter for current measure
- Oscillograph for wake-up time measure

5.2 Hardware setup

To measure the power consumption, remove R51 and connect the multimeter to JP2.

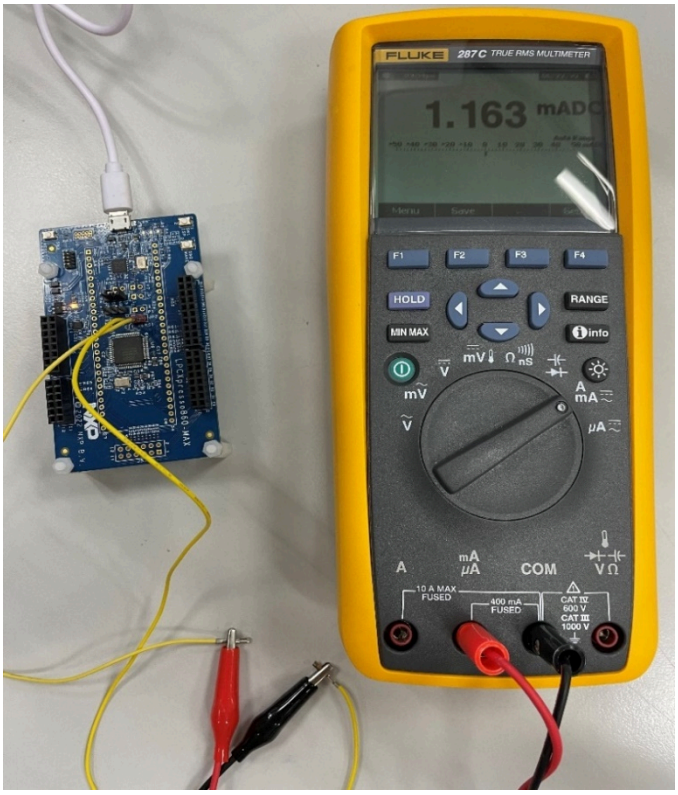

Figure 2. Hardware setup on LPCXpresso860-MAX EVK Board

5.3 Software environment setup

- MCUXpresso IDE v11.5.1_7266

- Serial terminal program, for example TeraTerm or Putty
- SDK_2_11_1_LPCXpresso860MAX

5.4 Reference software and hardware implementation

During the power consumption and wake-up time test, `uart0` is used to communicate with PC for test function select. In the test code, turn off the clock for `uart0` and any other unused peripherals after the test function is selected. It does not affect the power consumption.

To make the power consumption as little as possible, configure the test code and EVK as below:

- Code configuration:
  - Drive all the GPIO pin to low and output except the wake-up pin `PIO0_4`, reset pin `PIO0_5` and the pin used for wake-up time test.
  - Set the optimization level to highest for the wake-up time test
  - Set the Sleep mode/Deep sleep mode/Power-down mode wakeup test pin to output low in `PIN_INT0_IRQHandler()` and locate the ISR into RAM for wake-up time test
  - Set the Deep power-down mode wakeup test pin `PIO1_5` to output high in `ResetISR()`.
  - Disable BOD reset and power down BOD.
  - Power down the unused analog blocks.
  - Attach the clock of these unused peripherals to none.
- EVK modification:
  - Remove the R38, R39, R52, R60 to disconnect the on-board debugger to decrease the sink current.
  - Remove the R5, R6, R8 to disconnect the LED.
  - Remove the C20 for the Deep power-down mode wakeup time test when the wakeup source is reset pin.

5.5 Running and measure results

```
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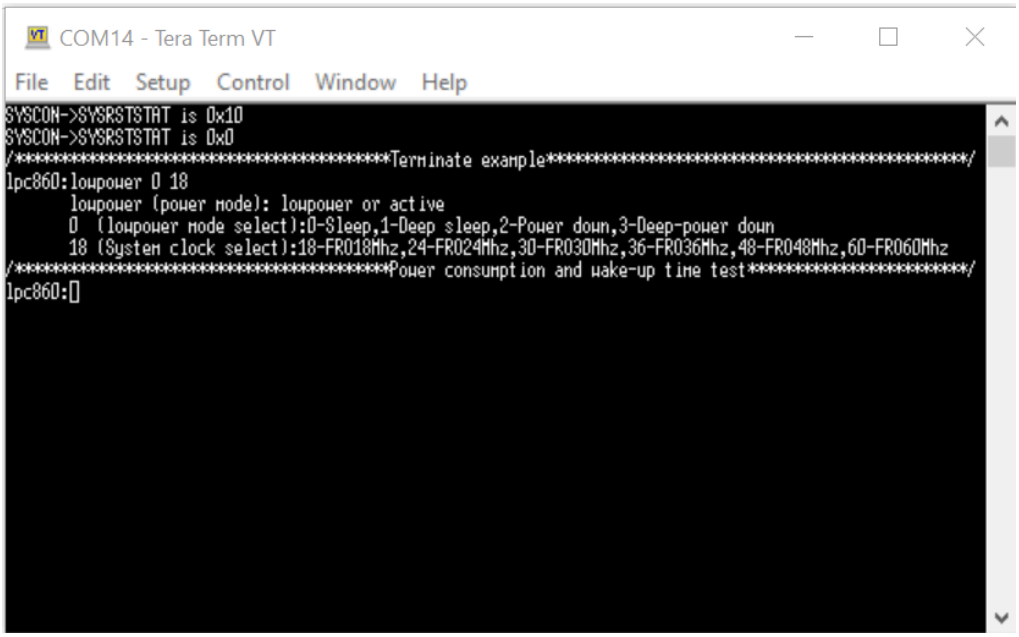

Figure 3. Power consumption test terminal

Note: *To use the USB to UART module to communicate with the device, disconnect the module when testing the power consumption. It may take some sink current to the device. And set the transmit format to CR+LF in terminate tool.*

Table 3. Power consumption

System clock in power mode	Sleep (mA) VDD = 3.3 V	Deep sleep (mA) VDD = 3.3 V	Power-down (uA) VDD = 3.3 V	Deep power-down (uA) VDD = 3.3 V
18 MHz	1.372	0.254	3.03	0.39
24 MHz	1.749	0.284	2.95	0.40
30 MHz	2.126	0.306	2.97	0.40
36 MHz	2.404	0.257	2.96	0.40
48 MHz	3.110	0.293	2.99	0.40
60 MHz	3.810	0.306	2.97	0.40

When testing the wake-up time, use the `PIO0_4` as the wake-up source for Sleep mode/Deep sleep mode/ Power-down mode and the `PIO1_6` to detect whether the chip is woken up. As shown in Figure 4, the wake-up time is from when the `PIO0_4` is triggered from high to low level to wake up the chip to when the `PIO1_6` is set to low. The channel 1 is `PIO1_6` and channel 2 is `PIO0_4`.

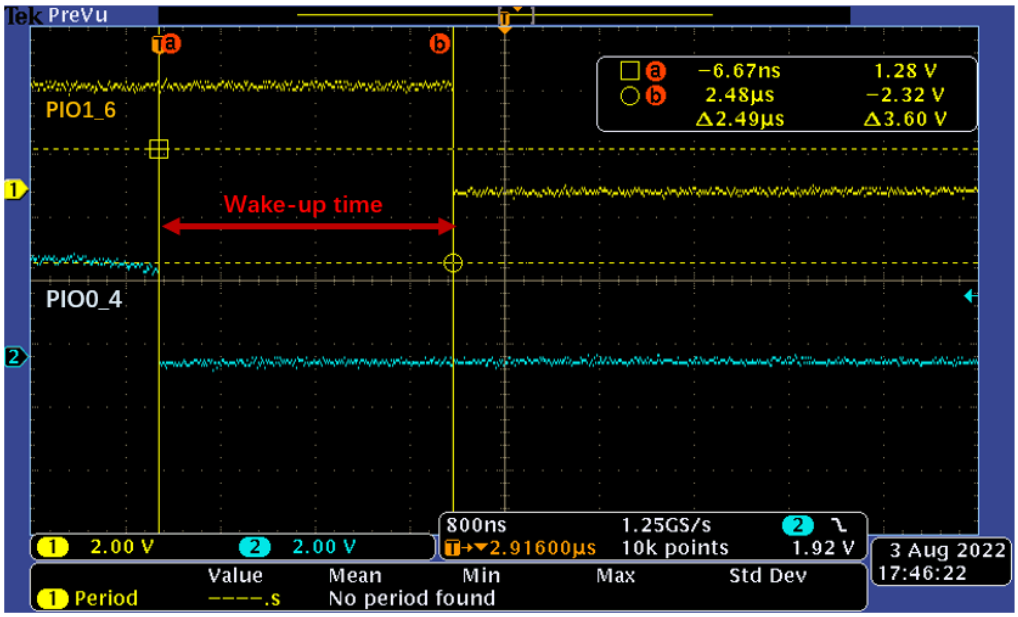

Figure 4. Wake-up time oscillator screen

When testing the wakeup time in the Deep power-down mode, use the reset pin `PIO0_5` as the wake up source and the `PIO1_5` to detect whether the chip is woken up in reset handler. As shown in Figure 5, wakeup time in the Deep power-down mode is measured from when the reset pin `PIO0_5` is triggered to from low to high level to wake up the chip, to when the `PIO1_5` is set to high. The channel 1 is `PIO1_5` and channel 2 is `PIO0_5`.

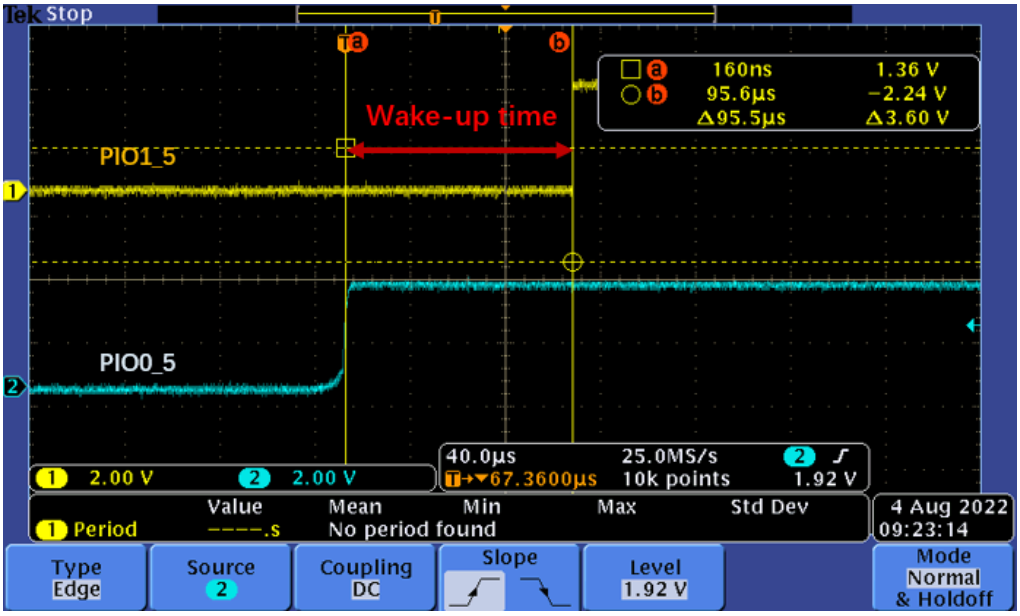

Figure 5. Wake-up time oscillator screen

Table 4. Wake-up time

Power mode System clock	Sleep (us) VDD = 3.3 V	Deep-sleep (us) VDD = 3.3 V	Power-down (us) VDD = 3.3 V	Deep Power-down (us) VDD = 3.3 V
18 MHz	2.49	3.39	49.07	97.3

Table 4. Wake-up time*...continued*

Power mode System clock	Sleep (us) VDD = 3.3 V	Deep-sleep (us) VDD = 3.3 V	Power-down (us) VDD = 3.3 V	Deep Power-down (us) VDD = 3.3 V
24 MHz	1.86	2.57	46.4	96.5
30 MHz	1.50	2.05	44.8	96.0
36 MHz	1.27	1.73	46.9	95.5
48 MHz	0.95	1.31	44.8	95.5
60 MHz	0.77	1.06	44.3	95.5

6 Revision history

Table 5 summarizes the revisions to this document.

Table 5. Revision history

Revision number	Date	Substantive changes
0	08 May 2023	Initial release

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