

BLDC Motor with Speed Closed Loop and DC-Bus Break Controller, driven by eTPU on MCF523x

Covers MCF523x and all eTPU-equipped Devices

by: Milan Brejl & Michal Princ
System Application Engineers
Roznov Czech System Center

This application note describes the design of a 3-phase brushless DC (BLDC) motor drive based on Freescale's ColdFire MCF523x microprocessor. The application design takes advantage of the enhanced time processing unit (eTPU) module, which is used as a motor control co-processor. The eTPU completely handles the motor control processing, eliminating the microprocessor overhead for other duties.

BLDC motors are very popular in a wide array of applications. Compared to a DC motor, the BLDC motor uses an electric commutator, replacing the mechanical commutator; thus making it more reliable than the DC motor. In BLDC motors, rotor magnets generate the rotor's magnetic flux, allowing BLDC motors to achieve higher efficiency. Therefore, BLDC motors may be used in high-end white goods (refrigerators, washing machines, dishwashers, etc.), high-end pumps, fans, and other appliances that require high reliability and efficiency.

The concept of the application is to create a speed-closed loop BLDC driver using a Hall position sensor. It serves as an example of a BLDC motor control system design using a Freescale microprocessor with the eTPU. It also

Table of Contents

1	ColdFire MCF523x and eTPU Advantages and Features	2
2	Target Motor Theory	4
3	System Concept	8
4	Software Design	18
5	Implementation Notes	44
6	Microprocessor Usage	48
7	Summary and Conclusions	49
8	References	49

illustrates the usage of dedicated motor control eTPU functions that are included in the DC motor control eTPU function set.

This application note also includes basic motor theory, system design concept, hardware implementation, and microprocessor and eTPU software design, including the FreeMASTER visualization tool.

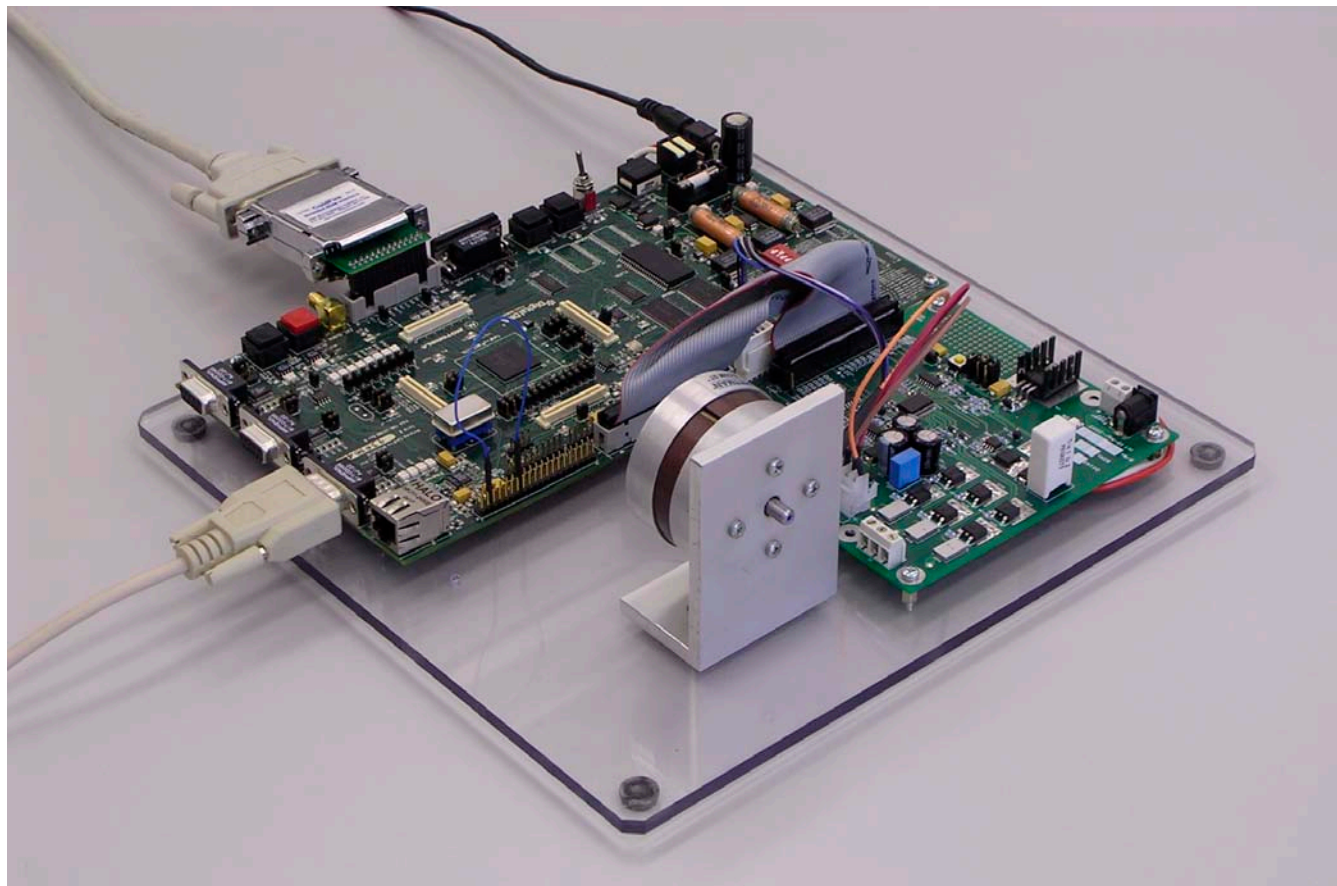


Figure 1. Using M523xEVB, 33395 Evaluation Motor Board, and Pittman BLDC Motor

1 ColdFire MCF523x and eTPU Advantages and Features

1.1 ColdFire MCF523x Microprocessor

The MCF523x is a family of highly-integrated, 32-bit microprocessors based on the V2 ColdFire core. It features a 16- or 32-channel eTPU, 64 Kbytes of internal SRAM, a 2-bank SDRAM controller, four 32-bit timers with DMA request capability, a 4-channel DMA controller, up to two CAN modules, three UARTs, and a queued SPI. The MCF523x family has been designed for general purpose industrial control applications. It is also a high-performance upgrade for users of the MC68332.

This 32-bit device is based on the Version 2 ColdFire reduced instruction set computer (RISC) core, operating at a core frequency of up to 150 MHz and a bus frequency of up to 75 MHz. On-chip modules include the following:

- V2 ColdFire core with an enhanced multiply-accumulate unit (EMAC) providing 144 Dhrystone 2.1MIPS @ 150 MHz
- eTPU with 16 or 32 channels, 6 Kbytes of code memory, and 1.5 Kbytes of data memory with eTPU debug support
- 64 Kbytes of internal SRAM
- External bus speed of half the CPU operating frequency (75 MHz bus @ 150 MHz core)
- 10/100 Mbps bus-mastering Ethernet controller
- 8 Kbytes of configurable instruction/data cache
- Three universal asynchronous receiver/transmitters (UARTs) with DMA support
- Controller area network 2.0B (FlexCAN module)
 - Optional second FlexCAN module multiplexed with the third UART
- Inter-integrated circuit (I2C) bus controller
- Queued serial peripheral interface (QSPI) module
- Hardware cryptography accelerator (optional)
 - Random number generator
 - DES/3DES/AES block cipher engine
 - MD5/SHA-1/HMAC accelerator
- 4-channel, 32-bit direct memory access (DMA) controller
- 4-channel, 32-bit input capture/output compare timers with optional DMA support
- 4-channel, 16-bit periodic interrupt timers (PITs)
- Programmable software watchdog timer
- Interrupt controller capable of handling up to 126 interrupt sources
- Clock module with phase locked loop (PLL)
- External bus interface module including a 2-bank synchronous DRAM controller
- 32-bit, non-multiplexed bus with up to 8 chip select signals that support page-mode FLASH memories

For more information, refer to Reference 1.

1.2 eTPU Module

The eTPU is an intelligent, semi-autonomous co-processor designed for timing control, I/O handling, serial communications, motor control, and engine control applications. It operates in parallel with the host CPU. The eTPU processes instructions and real-time input events, performs output waveform generation, and accesses shared data without the host CPU's intervention. Consequently, the host CPU setup and service times for each timer event are minimized or eliminated.

The eTPU has up to 32 timer channels, in addition to having 6 Kbytes of code memory and 1.5 Kbytes of data memory that store software modules downloaded at boot time, and can be mixed and matched as needed for any application.

The eTPU provides more specialized timer processing than the host CPU can achieve. This is partially due to the eTPU implementation, which includes specific instructions for handling and processing time events. In addition, channel conditions are available for use by the eTPU processor, thus eliminating many branches. The eTPU creates no host CPU overhead for servicing timing events.

For more information, refer to Reference 6.

2 Target Motor Theory

A brushless DC (BLDC) motor is a rotating electric machine where the stator is a classic three-phase stator, like that of an induction motor, and the rotor has surface-mounted permanent magnets (see Figure 2).

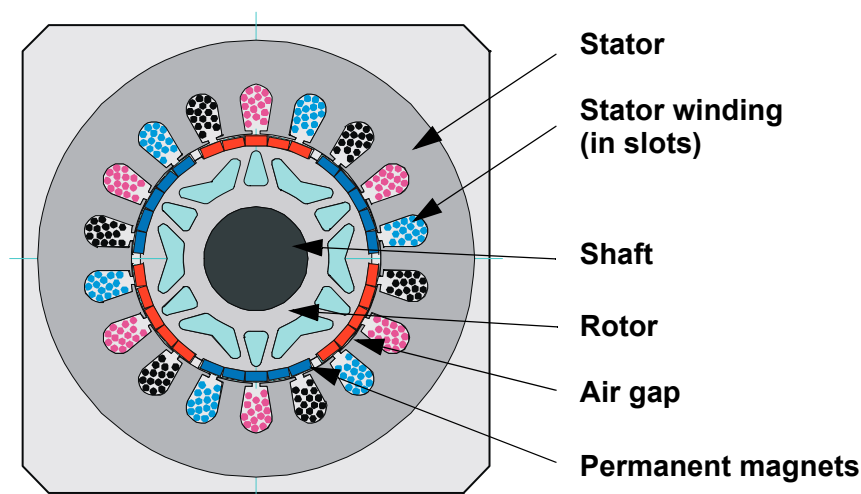


Figure 2. BLDC Motor - Cross Section

In this respect, the BLDC motor is equivalent to a reversed DC commutator motor, in which the magnet rotates while the conductors remain stationary. In the DC commutator motor, the current polarity is altered by the commutator and brushes. Unlike the brushless DC motor, the polarity reversal is performed by power transistors switching in synchronization with the rotor position. Therefore, BLDC motors often incorporate either internal or external position sensors to sense the actual rotor position, or the position can be detected without sensors.

2.1 Digital Control of a BLDC Motor

The BLDC motor is driven by rectangular voltage strokes coupled with the given rotor position (see Figure 3). The generated stator flux interacts with the rotor flux, which is generated by a rotor magnet and defines the torque and thus the speed of the motor. The voltage strokes must be properly applied to two phases of the three-phase winding system so that the angle between the stator flux and the rotor flux is kept as close to 90° as possible, to get the maximum generated torque. Therefore, the motor requires electronic control for proper operation.

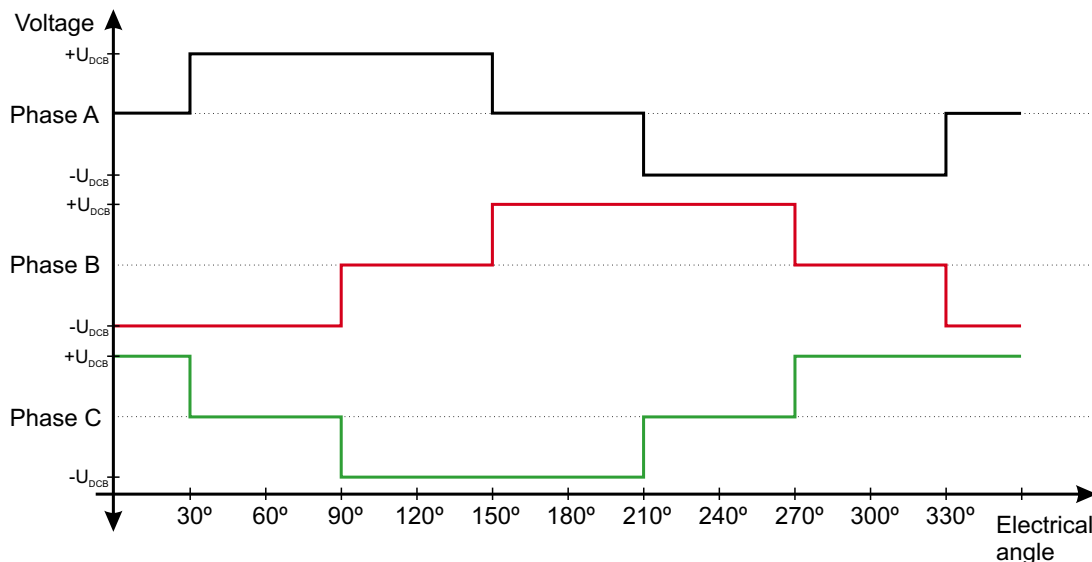


Figure 3. Voltage Strokes Applied to the 3-Phase BLDC Motor

For the common 3-phase BLDC motor, a standard 3-phase power stage is used (see [Figure 4](#)). The power stage utilizes six power transistors that operate in either an independent or complementary mode.

In both modes, the 3-phase power stage energizes two motor phases concurrently. The third phase is unpowered (see [Figure 3](#)). Thus, we get six possible voltage vectors that are applied to the BLDC motor using a pulse width modulation (PWM) technique (see [Figure 5](#)). There are two basic types of power transistor switching schemes: independent and complementary. Both switching modes are able to work in bipolar or unipolar mode. The presented application utilizes the complementary bipolar PWM mode.

For more information about PWM techniques, refer to Reference [15](#).

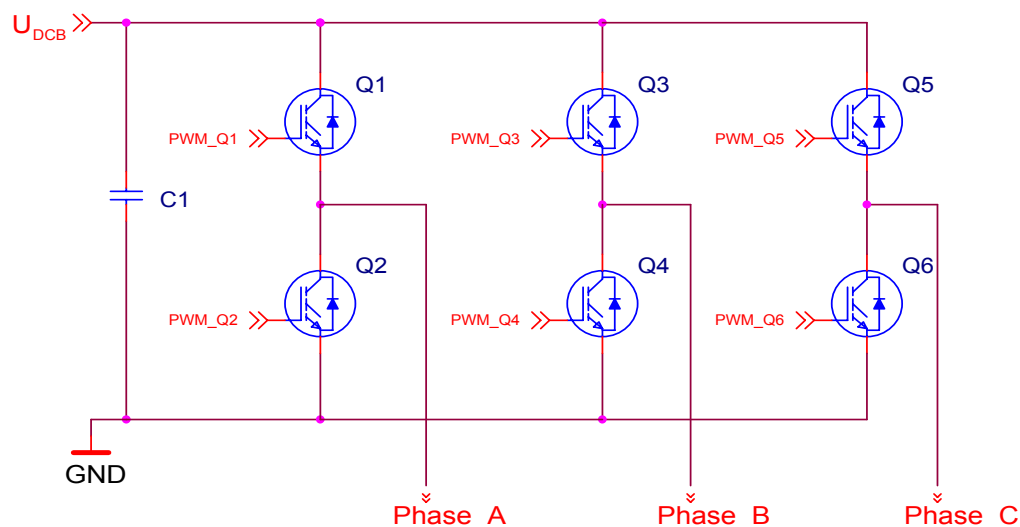


Figure 4. 3-Phase BLDC Power Stage

2.1.1 Commutation

Commutation provides the creation of a rotational field. As mentioned earlier, for proper operation of a BLDC motor, it is necessary to keep the angle between the stator and rotor flux as close to 90° as possible. We get a total of six possible stator flux vectors with a six-step control. The stator flux vector must be changed at specific rotor positions, which are usually sensed by the Hall sensors. The Hall sensors generate three signals that also consist of six states. Each of the Hall sensors' states correspond to a certain stator flux vector. All of the Hall sensors states, with corresponding stator flux vectors, are illustrated in Figure 5.

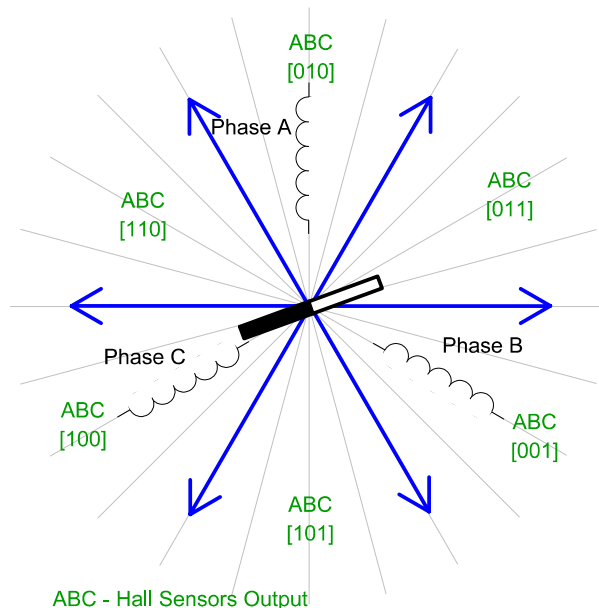


Figure 5. Stator Flux Vectors at Six-Step Control

The next two figures depict the commutation process. The actual rotor position in Figure 6 corresponds to the Hall sensors state ABC[110] (see Figure 5). Phase A is connected to the positive DC bus voltage by the transistor Q1; phase C is connected to the ground by transistor Q6, and phase B is unpowered.

As soon as the rotor reaches a certain position (see Figure 7), the Hall sensors state changes its value from ABC[110] to ABC[100]. A new voltage pattern is selected and applied to the BLDC motor.

As shown below, when using the six-step control technique, it is difficult to keep the angle between the rotor flux and the stator flux precisely at 90° in a six-step control technique. The actual angle varies from 60° to 120° .

The commutation process is repeated per each 60 electrical degrees and is critical to maintain its angular (time) accuracy. Any deviation causes torque ripples, resulting in speed variation.

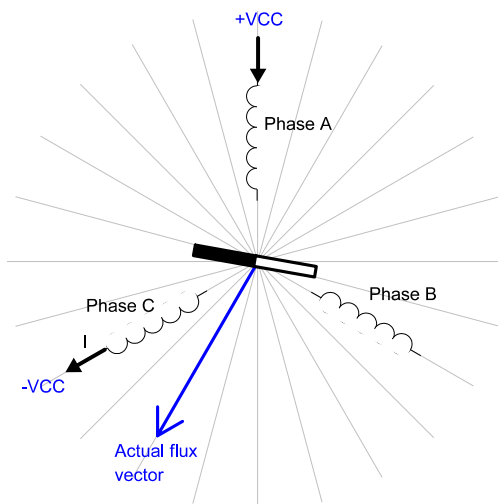


Figure 6. Situation Right Before Commutation (Counter-Clockwise Motion)

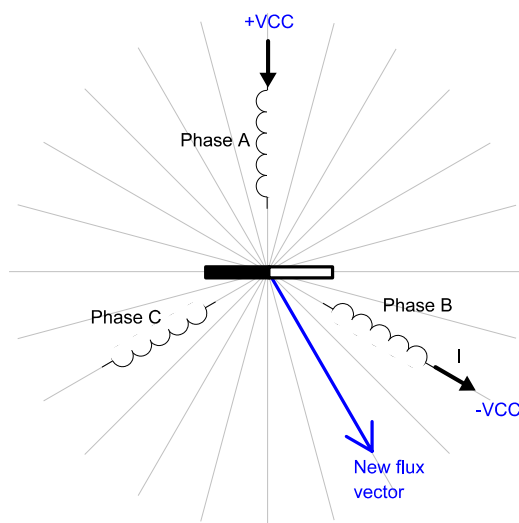


Figure 7. Situation Right After Commutation

2.1.2 Speed Control

Commutation ensures the proper rotor rotation of the BLDC motor, while the motor speed only depends on the amplitude of the applied voltage. The amplitude of the applied voltage is adjusted using the PWM technique. The required speed is controlled by a speed controller, which is implemented as a conventional proportional-integral (PI) controller. The difference between the actual and required speeds is input to the PI controller which then, based on this difference, controls the duty cycle of the PWM pulses that correspond to the voltage amplitude required to maintain the desired speed.

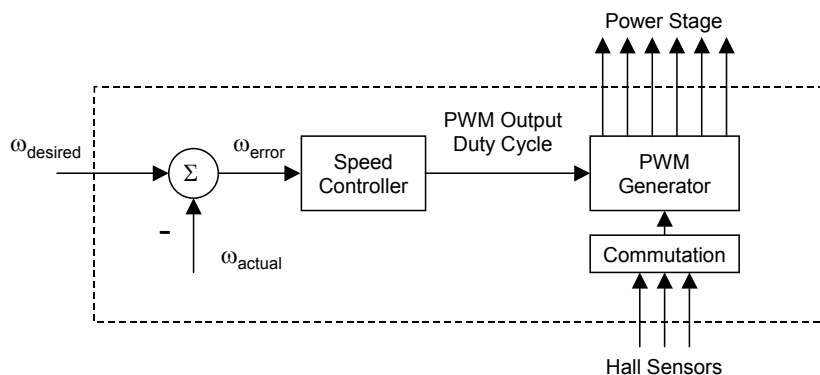


Figure 8. Speed Controller

The speed controller calculates the PI algorithm given in the equation below:

$$u(t) = K_c \left[e(t) + \frac{1}{T_I} \int_0^t e(\tau) d\tau \right]$$

After transforming the equation into a discrete time domain using an integral approximation with the Backward Euler method, we get the following equations for the numerical PI controller calculation:

$$u(k) = u_p(k) + u_I(k)$$

$$u_p(k) = K_c \cdot e(k)$$

$$u_I(k) = u_I(k-1) + K_c \frac{T}{T_I} \cdot e(k)$$

where:

$e(k)$	=	Input error in step k
$w(k)$	=	Desired value in step k
$m(k)$	=	Measured value in step k
$u(k)$	=	Controller output in step k
$u_p(k)$	=	Proportional output portion in step k
$u_I(k)$	=	Integral output portion in step k
$u_I(k-1)$	=	Integral output portion in step k-1
T_I	=	Integral time constant
T	=	Sampling time
K_c	=	Controller gain

3 System Concept

3.1 System Outline

The system is designed to drive a 3-phase BLDC motor. The application meets the following performance specifications:

- Voltage control of a BLDC motor using Hall sensors
- Targeted at ColdFire MCF523x evaluation board (M523xEVB), 33395 evaluation motor board, and Pittman BLDC motor (N2311)

- Control technique incorporates:
 - Voltage BLDC motor control with speed-closed loop
 - Both directions of rotation
 - 4-quadrant operation
 - Start from any motor position without rotor alignment
 - Minimum speed of 300 RPM
 - Maximum speed of 10000 RPM (limited by power supply)
- Manual interface (start/stop switch, up/down push button control, LED indication)
- FreeMASTER control interface (speed set-up)
- FreeMASTER monitor
 - FreeMASTER graphical control page (required speed, actual motor speed, start/stop status, fault status)
 - FreeMASTER speed scope (observes required, ramp, and actual speeds)
 - FreeMASTER Hall sensors scope (observes actual Hall sensors state, motor direction, and revolution counter)
- DC bus over-current fault protection
- DC bus over-voltage protection

3.2 Application Description

A standard system concept is chosen for the motor control function (see [Figure 9](#)). The system incorporates the following hardware:

- Evaluation board M523xEVB
- 33395 evaluation motor board
- Pittman BLDC motor (N2311) with Hall sensors
- Power supply 9V DC, 2.7Amps

The eTPU module runs the main control algorithm. The 3-phase PWM output signals for a 3-phase inverter are generated according to feedback signals from Hall sensors and the input variable values, provided by the microprocessor CPU.

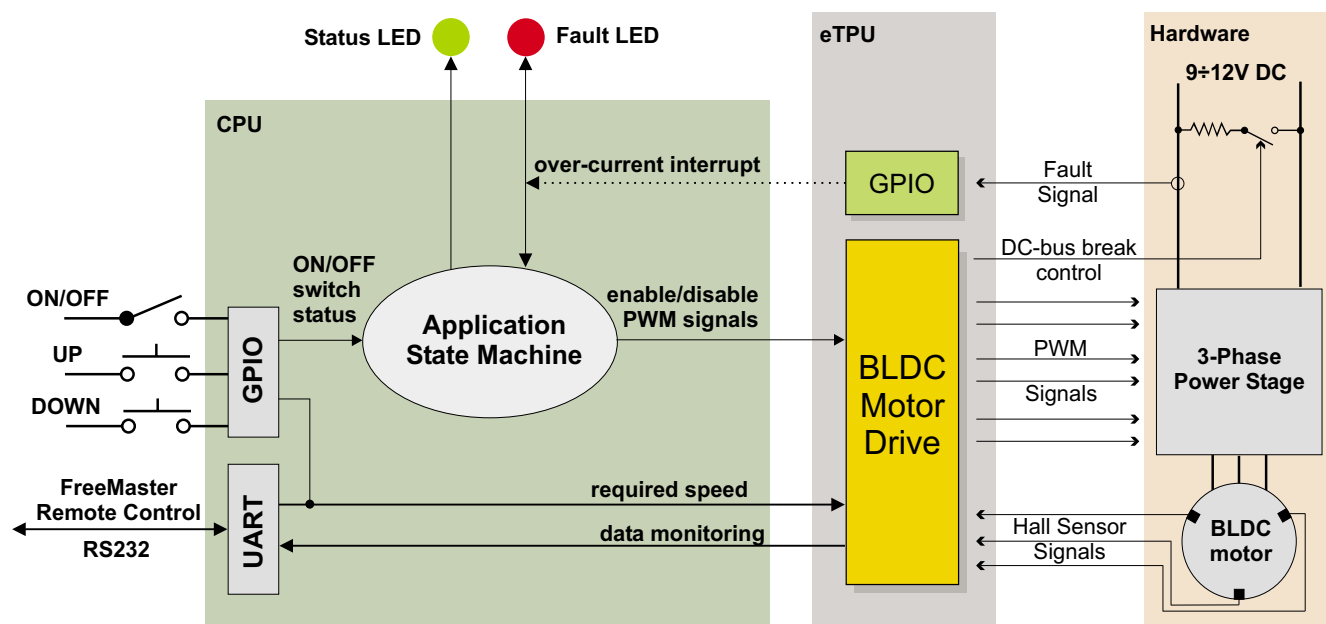


Figure 9. System Concept

The system processing is distributed between the CPU and the eTPU, which both run in parallel.

The CPU performs the following tasks:

- Periodically scans the user interface (ON/OFF switch, up and down buttons, FreeMASTER). Based on the user input, it handles the application state machine and calculates the required speeds, which is passed to the eTPU.
- Periodically reads application data from ETPU DATA RAM in order to monitor application variables.
- In the event of an overcurrent fault, the PWM outputs are immediately temporarily disabled by the eTPU hardware. Then, after an interrupt latency, the CPU disables the PWM outputs permanently and displays the fault state.

The eTPU performs the following tasks:

- Six eTPU channels (PwMC) are used to generate PWM output signals.
- Three eTPU channels (HD) are used to process Hall sensor signals. On each incoming edge, a revolution period is calculated and the PWM output signals are commuted.
- One eTPU channel (BC) is used for controlling the DC-bus break.
- One eTPU channel (GPIO) is used to generate an interrupt to the CPU when the over-current fault signal activates.
- eTPU controls a speed closed loop. The actual motor speed is calculated based on the revolution period and compared with the required speed, provided by the CPU and passed through a ramp. The speed PI control algorithm processes the error between the required and actual speed. The PI controller output is passed to the PWM generator as a newly corrected value of the applied motor voltage.

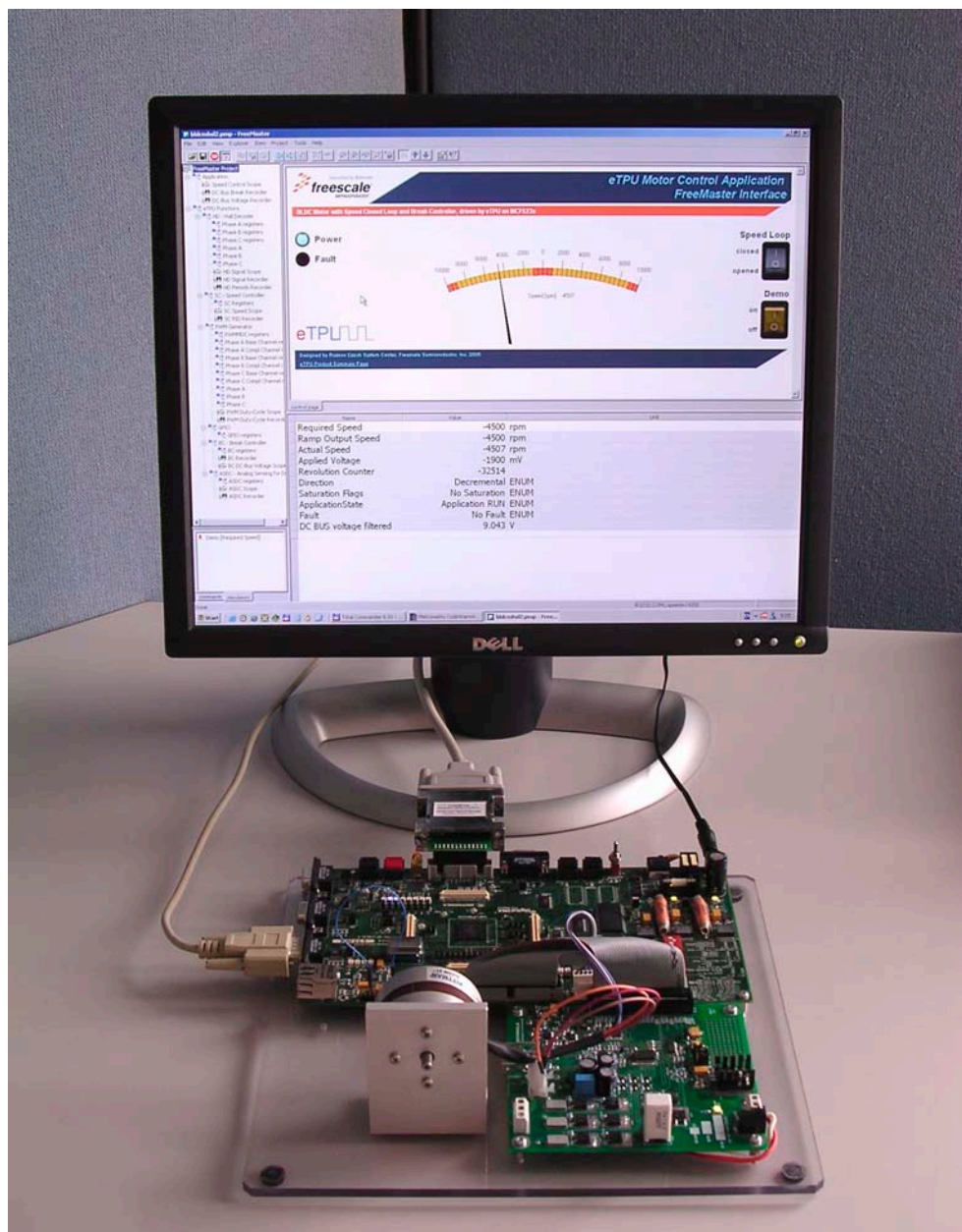


Figure 10. The Application and FreeMASTER Screen

3.2.1 User Interface

The application is interfaced by the following:

- ON/OFF switch on M523xEVB
- Up/down buttons on M523xEVB, or
FreeMASTER running on a PC connected to the M523xEVB via an RS232 serial cable

The ON/OFF switch affects the application state and enables and disables the PWM phases. When the switch is in the off-position, no voltage is applied to the motor windings. When the ON/OFF switch is in

System Concept

the on-position, the motor speed can be controlled either by the up and down buttons on the M523xEVB, or by the FreeMASTER on the PC. The FreeMASTER also displays a control page, real-time values of application variables, and their time behavior using scopes.

FreeMASTER software was designed to provide an application-debugging, diagnostic, and demonstration tool for the development of algorithms and applications. It runs on a PC connected to the M523xEVB via an RS232 serial cable. A small program resident in the microprocessor communicates with the FreeMASTER software to return status information to the PC and process control information from the PC. FreeMASTER software, executing on a PC, uses part of Microsoft Internet Explorer as the user interface.

Note, that FreeMASTER version 1.2.31.1 or higher is required. The FreeMASTER application can be downloaded from <http://www.freescale.com>. For more information about FreeMASTER, refer to Reference 5.

3.3 Hardware Implementation and Application Setup

As previously stated, the application runs on the MCF523x family of ColdFire microprocessors using the following:

- M523xEVB
- 33395 evaluation motor board
- 3-Phase Pittman BLDC motor (N2311)
- Power supply, 9-12V DC, minimum 2.7Amps

Figure 11 shows the connection of these parts. All system parts are supplied by Freescale and documented according to references.

3.3.1 ColdFire MCF523x Evaluation Board (M523xEVB)

The EVB is intended to provide a mechanism for customers to easily evaluate the MCF523x family of ColdFire microprocessors. The heart of the evaluation board is the MCF5235; all other M523x family members have a subset of the MCF5235 features and can therefore be fully emulated using the MCF5235 device.

The M523xEVB is fitted with a single 512K x 16 page-mode Flash memory (U19), giving a total memory space of 2 Mbytes. Alternatively, a footprint is available for upgrading flash to a 512K x 32 page-mode Flash memory (U35), doubling the memory size to 4 Mbytes.

For more information, refer to Reference 2.

Table 1 lists all M523xEVB jumper settings used in the application.

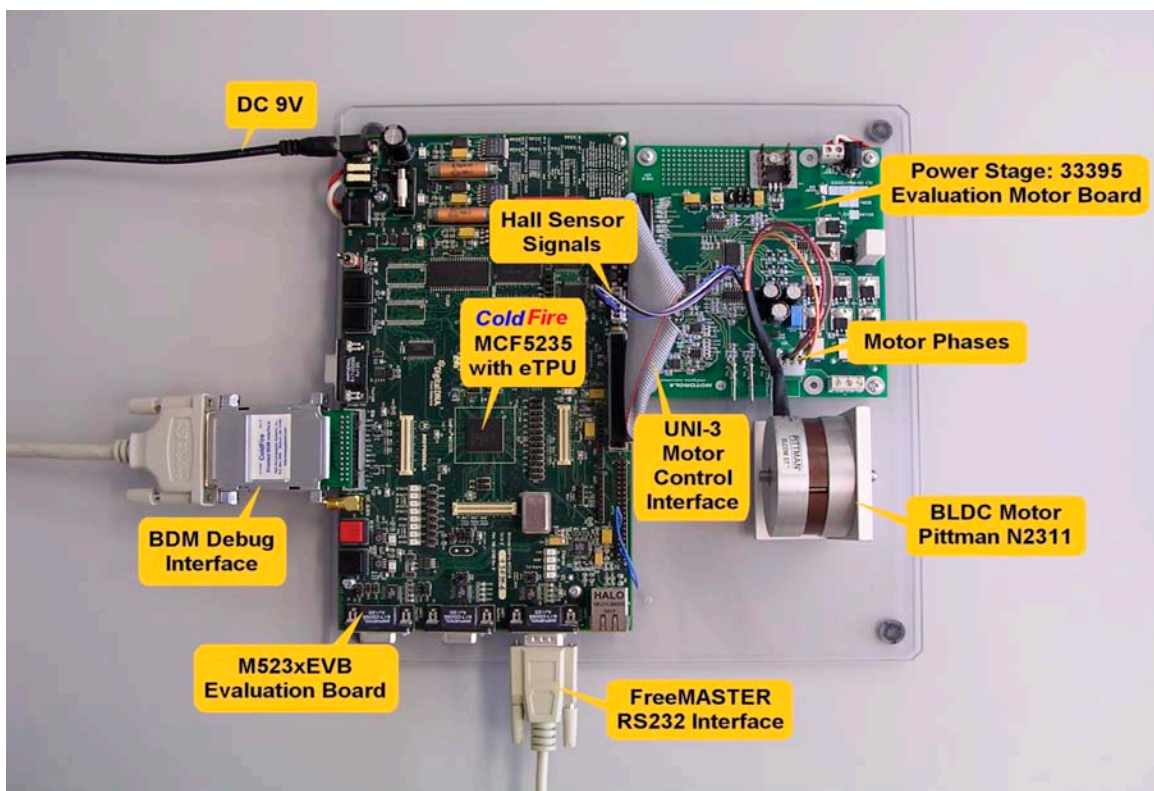


Figure 11. Connection of Application Parts

Table 1. M523xEVB Jumper Settings

Jumper	Setting	Jumper	Setting	Jumper	Setting	Jumper	Setting
JP1	1 2	JP20	1 2-3	JP40	1-2	JP60	1-2
JP2	1-2	JP21	1 2-3	JP41	1-2	JP61	1-2
JP3	1 2	JP22	1 2-3	JP42	1-2	JP62	1 2
JP4	1-2	JP23	1 2-3	JP43	1-2	JP63	1 2
JP5	1 2-3	JP24	1 2-3	JP44	1-2	JP64	1 2-3
JP6	1-2 3	JP25	1-2 3	JP45	1-2	DIP1	ON
JP7	1 2-3	JP26	1-2 3	JP46	1-2	DIP2	ON
JP8	1-2 3	JP27	1-2	JP47	1-2	DIP3	ON
JP9	1 2-3	JP28	1-2	JP48	1-2	DIP4	ON
		JP29	1-2	JP49	1-2	DIP5	ON
JP10	1 2-3	JP30	1-2	JP50	1-2 3	DIP6	ON
JP11	1 2-3	JP31	1 2-3	JP51	1-2 3	DIP7	OFF
JP12	1 2-3	JP32	1-2 3	JP52	1-2 3	DIP8	ON
JP13	1 2-3	JP33	1-2	JP53	1 2	DIP9	ON
JP14	1 2-3	JP34	1-2	JP54	1 2	DIP10	ON
JP15	1 2-3	JP35	1-2 3	JP55	1 2	DIP11	OFF
JP16	1 2-3	JP36	1-2 3	JP56	1-2 3	DIP12	ON
JP17	1 2-3	JP37	1-2	JP57	1-2		
JP18	1 2-3	JP38	1-2	JP58	1-2		
JP19	1 2-3	JP39	1-2	JP59	1-2		

BLDC Motor with Speed Closed Loop and DC-Bus Break Controller, driven by eTPU on MCF523x, Rev. 0

3.3.2 Flashing the M523xEVB

The CFFlasher utility can be used for programming code into the FLASH memory on the MCF523xEVB. Check for correct setting of switches and jumpers: SW7-6 on, SW7-7 off, JP64 2-3, (JP31 2-3). The flashing procedure is as follows:

1. Run Metrowerks CodeWarrior for ColdFire and open the project. Choose the simple_elflash target and compile the application. A file simple_elflash.elf.S19, which will be loaded into FLASH memory, is created in the project directory bin.
2. Run the CFFlasher application, click on the Target Config button. In the Target Configuration window select the type of board as M523xEVB and the BDM Communication as PE_LPT (see Figure 12). Click OK to close the window.
3. Go to the Program section by clicking the Program button. Select the simple_elflash.elf.S19 file and check the Verify after Program option (see Figure 13). Finally, press the Program button at the bottom of the window to start loading the code into the FLASH memory.
4. If the code has been programmed correctly, remove the BDM interface and push the RESET button on the M523xEVB. The application should now run from the FLASH.

The CFFlasher application can be downloaded from <http://www.freescale.com/coldfire>.

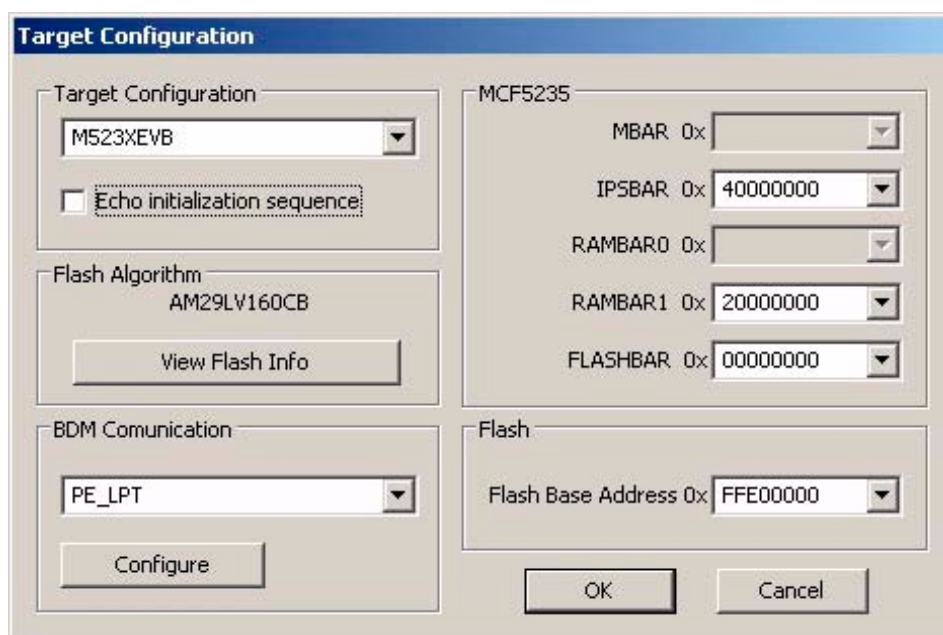


Figure 12. CFFlasher Target Configuration Window

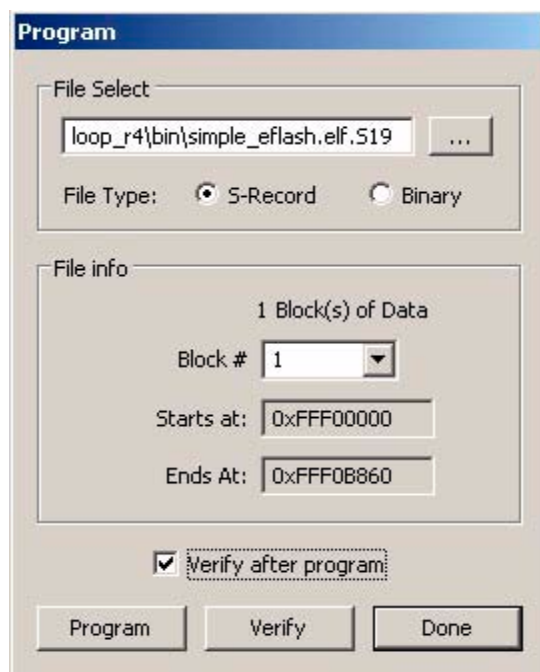


Figure 13. CFFlasher Program Window

3.3.3 Setting Overcurrent Level

The over-current fault signal is connected to the eTPU output disable pin (LETPUODIS) that handles eTPU hardware faults, along with the proper eTPU configuration. This connection is part of M523xEVB¹. In order to enable handling of the fault by software, the fault signal, available on the LETPUODIS pin, must be connected to eTPU channel 4, which runs the GPIO function and generates an interrupt request to the CPU in the case of a fault. This connection must be done manually. Connect pin 6 (LETPUODIS) with pin 16 (ETPUCH4) on the eTPU header (see Figure 14).

The over-current level is set by trimmer R41 on M523xEVB (see Figure 15). Reference 3 describes what voltage the trimmer defines for the over-current comparator. Follow the steps below to set up the over-current level properly without measuring the voltage:

1. Connect all system parts according to Figure 11, connect pin 16 with pin 40 on the eTPU header. Now the over-current interrupt is disabled. The over-current fault is handled by hardware only.
2. Download and start the application.
3. Turn the ON/OFF switch ON. Using the up and down buttons, set the required speed to the maximum.
4. Adjust the R41 trimmer. You can find a level from which the red LED starts to light and the motor speed starts to be limited. Set the trimmer level somewhat higher, so that the motor can run at the maximum speed.
5. Turn the ON/OFF switch OFF.

1. When the eTPU is configured for 32-channels, LTPUODIS is applicable to channels 0-15. When the ethernet is enabled (SW11 on), the function of LTPUODIS then changes to channels 0-7 and UTPUODIS thus controls channels 8-15. Therefore the UTPUODIS must be tied to LTPUODIS to enable the application to work when ethernet is enabled.

System Concept

6. Connect pin 16 with pin 6 on the eTPU header. Now the over-current interrupt is enabled. The over-current fault is handled by both hardware and software.
7. Turn the ON/OFF switch ON. Using the up and down buttons, set the required speed to the maximum.

If the application goes to the fault state during the acceleration, adjust the R41 trimmer level somewhat higher, so that the motor can get to the maximum speed.

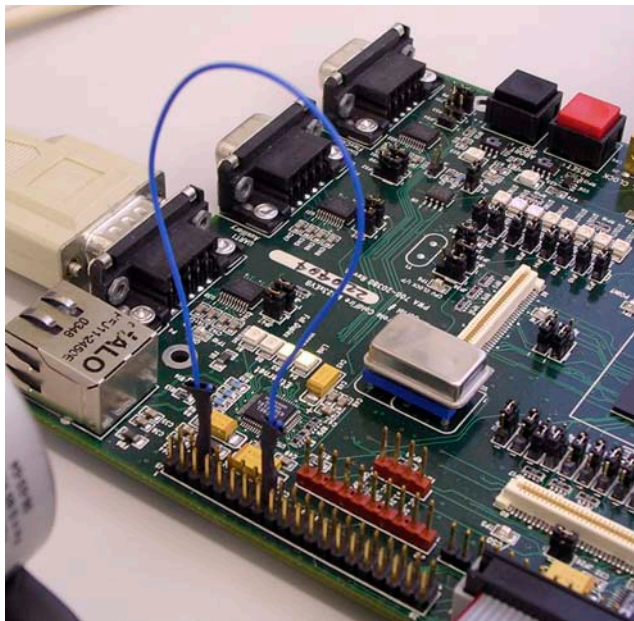


Figure 14. Connection Between UETPUODIS, LETPUODIS, and ETPUCH4 on the eTPU Header

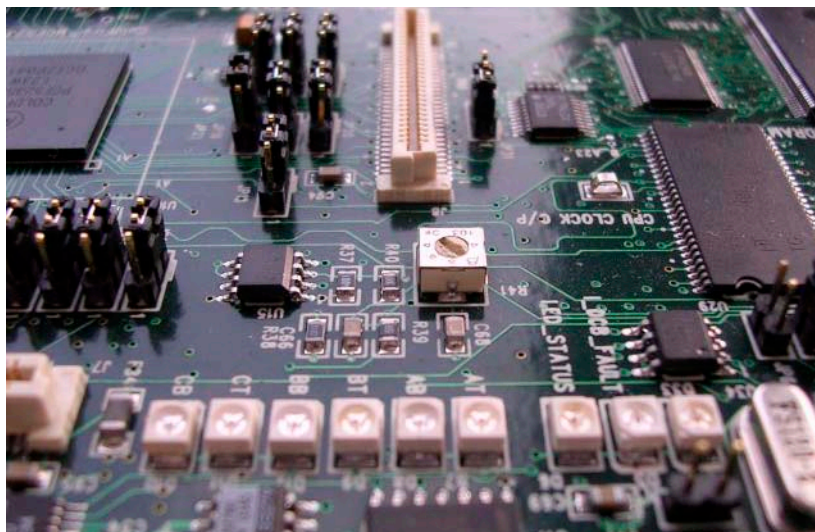


Figure 15. Overcurrent Level Trimmer on M523xEVB (R41)

3.3.4 33395 Evaluation Motor Board

The 33395 evaluation motor board is a 12-volt, 8-amp power stage, which is supplied with a 40-pin ribbon cable. In combination with the M523xEVB, it provides an out-of-the-box software development platform

for small brushless DC motors. The power stage enables sensing a variety of feedback signals suitable for different motor control techniques. It measures all the three phase currents, reconstructs the DC-bus current from them, the DC-bus voltage, and the Back-EMF voltages with zero cross sensing. All the analog signals are adapted to be directly sampled by the A/D converter. This single-board power stage contains an analog bridge gate driver integrated circuitry, sensing and control circuitry, power N-MOSFET transistors, DC-bus break chopper, as well as various interface connectors for the supply and the motor.

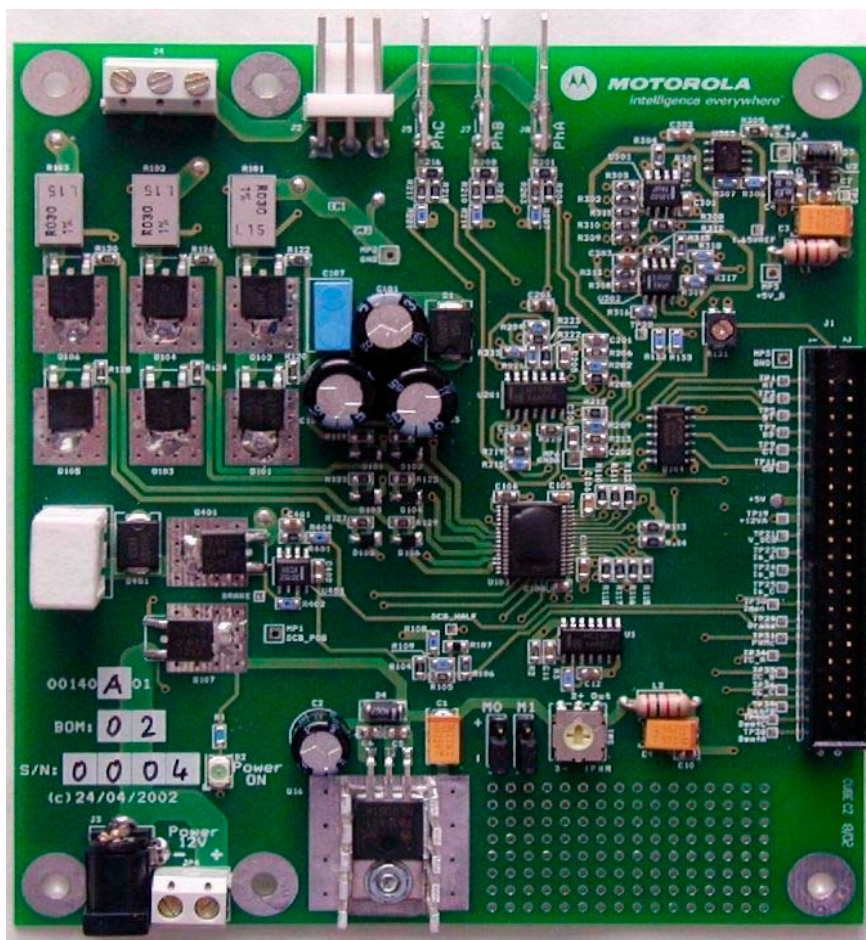


Figure 16. 33395 Evaluation Motor Board

For more information, refer to Reference 3.

3.3.5 BLDC Motor with Hall Sensors

The enclosed motor is a low-voltage Pittman BLDC motor (N2311). The motor is capable of being controlled by Hall sensor techniques. The motor characteristics in Table 2 apply to operation at 25°C.

Figure 34 depicts the motor timing. For more motor specifications, refer to Reference 4.

Table 2. Pittman BLDC Motor (N2311) Motor Characteristics

Characteristic	Symbol	Min	Type	Max	Units
Reference Winding Voltage	V_t	—	—	9.6	V
Speed @ V_t		—	—	12000	RPM
Torque Constant	K_t	—	0.007	—	Nm/A
	K_t	—	1.082	—	oz-in/A
Voltage Constant	K_e	—	0.8	—	V/kRPM
Terminal Resistance	R_t	0.13	—	0.18	W
Winding Inductance	L	—		—	mH
Continuous Current	I_{cs}	—	—	9.96	A
No Load Current @ V_t	I_{ps}	—	1.20	—	A
Number of Poles	J_m	—	8	—	—
Temperature Rating		-10	—	80	
		14	—	176	

3.3.6 Power Supply

The power supply supplied with the M523xEVB, 9.0V/2.7A, is also used to power the 33395 evaluation motor board. The application is scaled for this 9V power supply. In case a 12V power supply is used instead, the application should be rescaled for the wider voltage and speed range.

4 Software Design

This section describes the software design of the BLDC motor drive application. The system processing is distributed between the CPU and the eTPU, which run in parallel. The CPU and eTPU tasks are described in terms of the following:

- CPU
 - Software flowchart
 - Application state diagram
 - eTPU application API
- eTPU
 - eTPU block diagram
 - eTPU timing

The CPU software uses several ready-to-use Freescale software drivers. The communication between the microprocessor and the FreeMASTER on a PC is handled by software included in `fmaster.c/.h` files. The eTPU module uses the general eTPU utilities, eTPU function interface routines (eTPU function API), and eTPU application interface routines (eTPU application API). The general utilities, included in the `etpu_util.c/.h` files, are used for initialization of global eTPU module and engine settings. The eTPU function API routines are used for initialization of the eTPU channels and interfacing each eTPU function during run-time. An eTPU application API encapsulates several eTPU function APIs. The use of an eTPU application API eliminates the need to initialize each eTPU function separately and to handle all eTPU function initialization settings, and so ensures the correct cooperation of eTPU functions.

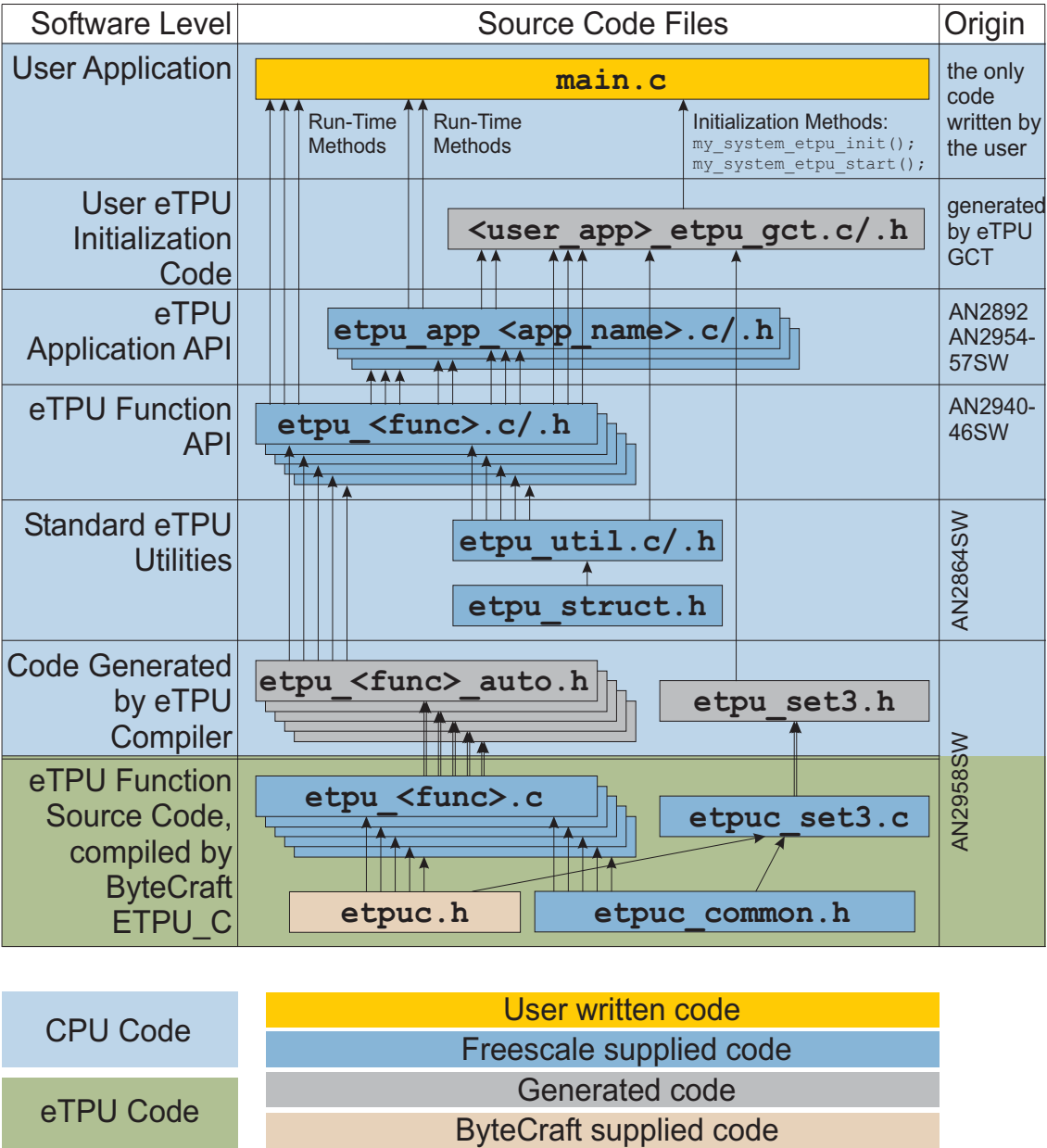


Figure 17. eTPU Project Structure

4.1 CPU Software Flowchart

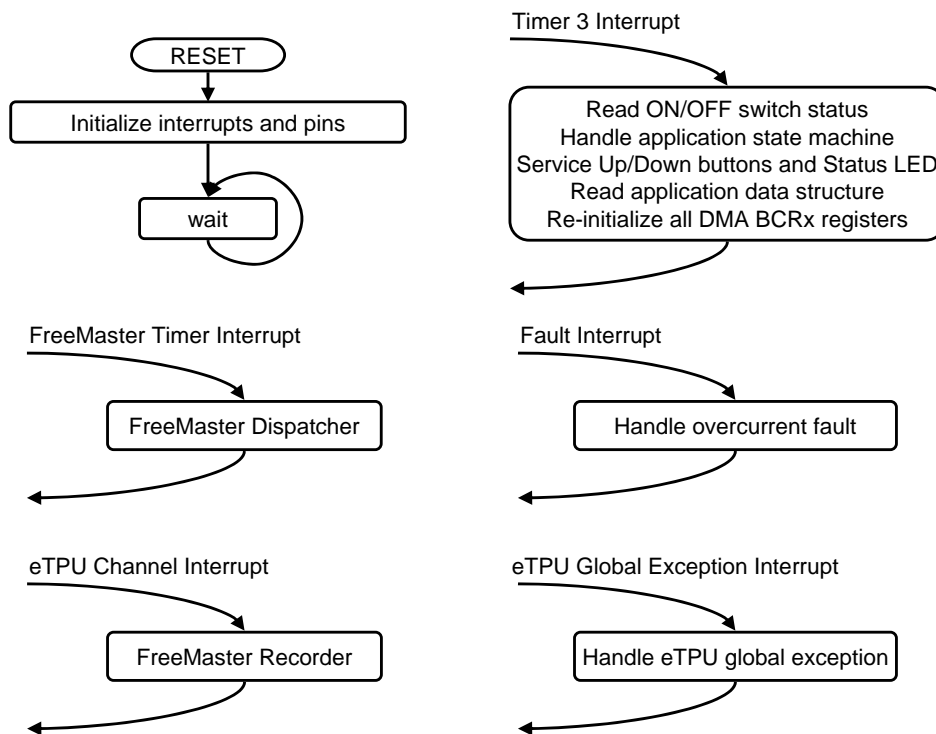


Figure 18. CPU Software Flowchart

After reset, the CPU software initializes peripherals, interrupts, and pins, and starts the eTPU module. At this point, the CPU and the eTPU run in parallel. The following CPU processing is incorporated in two periodic timer interrupts and one fault interrupt.

4.1.1 Initialization of Interrupts and Pins

The initialization of timer 3, eTPU channel 4 and 7 interrupts, and the eTPU global exception interrupt, together with initialization of the GPIO and LETPUODIS pins, is done by the `InitInterruptsAndPins` function.

4.1.2 Timer 3 Interrupt Service Routine

The timer 3 interrupt is handled by the `timer3_isr` function. The following actions are performed periodically, in `timer3_isr`:

- Read the ON/OFF switch status
- Handle the application state machine
The application state diagram is described in detail below.
- Service the up and down buttons and the status LED by the `ApplicationButtonsAndStatusLed` function

- Read the data structure through the eTPU application API routine `fs_etpu_app_bldcmhsl2_get_data` (see 4.3)
- Re-initialize all DMA BCRx registers in order to ensure the continuous operation of the DMA channels (see 4.4.5)

4.1.3 FreeMASTER Interrupt Service Routine

The FreeMASTER interrupt service routine is called `fmasterDispatcher`. This function is implemented in `fmaster.c`.

4.1.4 eTPU Channel Interrupt Service Routine

This interrupt, which is raised every PWM period by the PWMMDC eTPU function running on eTPU channel 7, is handled by the `etpu_ch7_isr` function. This function calls `fmasterRecorder`, implemented in `fmaster.c`, enabling the configuration of application variable time courses with a PWM-period time resolution.

4.1.5 Fault Interrupt Service Routine

The over-current fault interrupt, which is raised by the GPIO eTPU function running on eTPU channel 4, is handled by the `etpu_ch4_isr` function. The following actions are performed in order to switch the motor off:

- Reset the required speed
- Disable the generation of PWM signals
- Switch the fault LED on
- Enter `APP_STATE_MOTOR_FAULT`
- Set `FAULT_OVERCURRENT`

4.1.6 eTPU Global Exception Interrupt Service Routine

The global exception interrupt is handled by the `etpu_globalexception_isr` function. The following situations can cause this interrupt assertion:

- Microcode global exception is asserted.
- Illegal instruction flag is asserted.
- SCM MISC flag is asserted.

The following actions are performed in order to switch the motor off:

- Reset the required speed
- Disable the generation of PWM signals
- Enter `APP_STATE_GLOBAL_FAULT`
- Based on the eTPU global exception source, set `FAULT_MICROCODE_GE`, `FAULT_ILLEGAL_INSTR`, or `FAULT_MISC`

4.2 Application State Diagram

The application state diagram consists of seven states (see Figure 19). After reset, the application goes first to APP_STATE_INIT. Where the ON/OFF switch is in the OFF position, the APP_STATE_STOP follows; otherwise, the APP_STATE_MOTOR_FAULT is entered and the ON/OFF switch must be turned OFF to get from APP_STATE_MOTOR_FAULT to APP_STATE_STOP. Then the cycle between APP_STATE_STOP, APP_STATE_ENABLE, APP_STATE_RUN, and APP_STATE_DISABLE can be repeated, depending on the ON/OFF switch position. APP_STATE_ENABLE and APP_STATE_DISABLE states are introduced in order to ensure the safe transitions between the APP_STATE_STOP and APP_STATE_RUN states. Where the over-current fault interrupt is raised (see red line on Figure 19), the APP_STATE_MOTOR_FAULT is entered. This fault is cleared by moving the ON/OFF switch to the OFF position and thus entering the APP_STATE_STOP. Where the eTPU global exception interrupt is raised (see gray line on Figure 19), the APP_STATE_GLOBAL_FAULT is entered. The global fault is cleared by moving the ON/OFF switch to the OFF position and thus entering the APP_STATE_INIT.

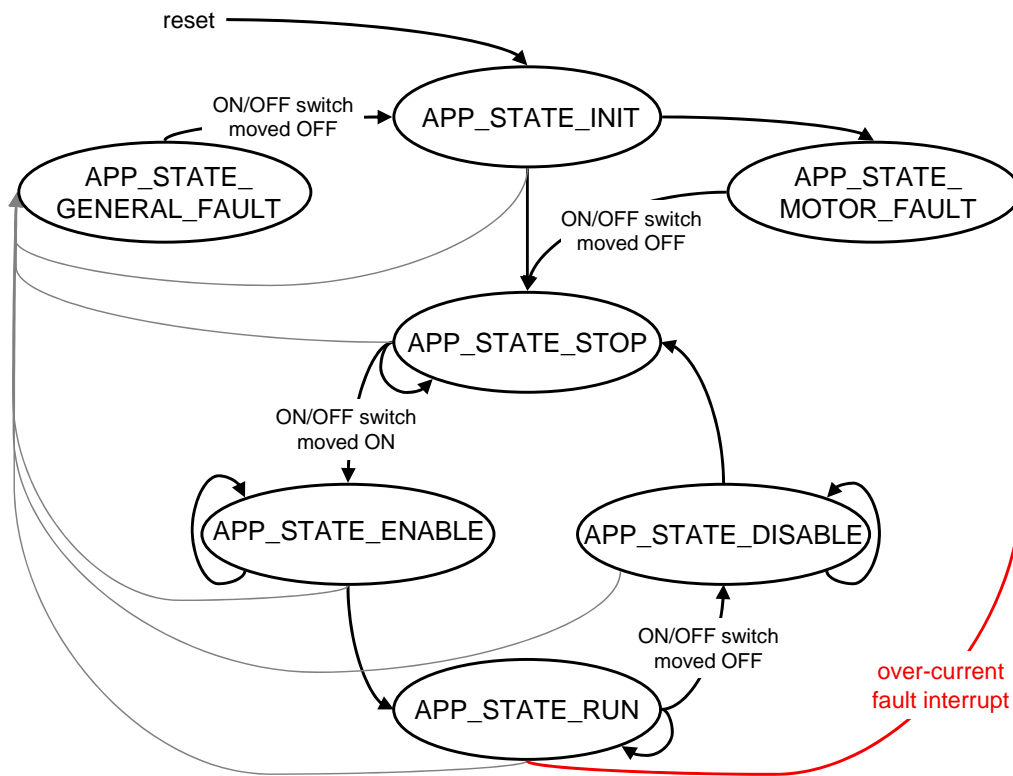


Figure 19. Application State Diagram

The following paragraphs describe the processing in each of the application states.

4.2.1 APP_STATE_INIT

This state is passed through only. It is entered either after a reset, or after the APP_STATE_GLOBAL_FAULT. The following actions are performed in order to initialize (re-initialize) the application:

- Call `my_system_etpu_init` routine for eTPU module initialization
- Get eTPU functions DATA RAM addresses for FreeMASTER
- Get the addresses of channel configuration registers for FreeMASTER
- Initialize QSPI & ADC
- Initialize DMA0-3 channels & DMA Timer 0
- Initialize the UART for FreeMASTER
- Initialize FreeMASTER
- Call `my_system_etpu_start` routine for eTPU Start. At this point, the CPU and the eTPU run in parallel.
- Depending on the ON/OFF switch position, enter `APP_STATE_STOP` or `APP_STATE_MOTOR_FAULT`

4.2.1.1 Initialization and Start of eTPU Module

The eTPU module is initialized using the `my_system_etpu_init` function. Later, after initialization of all other peripherals, the eTPU is started by `my_system_etpu_start`. These functions use the general eTPU utilities and eTPU function API routines. Both the `my_system_etpu_init` and `my_system_etpu_start` functions, included in `bldcmhsl2_etpu_gct.c` file, are generated by eTPU graphical configuration tool. The eTPU graphical configuration tool can be downloaded from http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=eTPU. For more information, refer to Reference 14.

The `my_system_etpu_init` function first configures the eTPU module and motor settings. Some of these settings include the following:

- Channel filter mode = three-sample mode
- Channel filter clock = `etpuclk` div 32

The input signals (from Hall sensors) are filtered by channel filters. The filter settings guarantee filtering all noise pulses up to a width of 853ns and pass pulses from a width of 1.28μs (at 150 MHz system clock).

- TCR1 source = `etpuclk` div 2
- TCR1 prescaler = 1

The TCR1 internal eTPU clock is set to its maximum rate of 37.5 MHz (at 150 MHz system clock), corresponding to the 27ns resolution of generated PWM signals.

- TCR2 source = `etpuclk` div 8
- TCR2 prescaler = 12

The TCR2 internal eTPU clock is set to a rate of 781.25 kHz (at 150 MHz system clock). The TCR2 clock settings are optimized for motor speed calculation precision.

After configuring the module and engine settings, the `my_system_etpu_init` function initializes the eTPU channels.

- Channel 1 - Hall decoder (HD) - Phase A
- Channel 2 - Hall decoder (HD) - Phase B

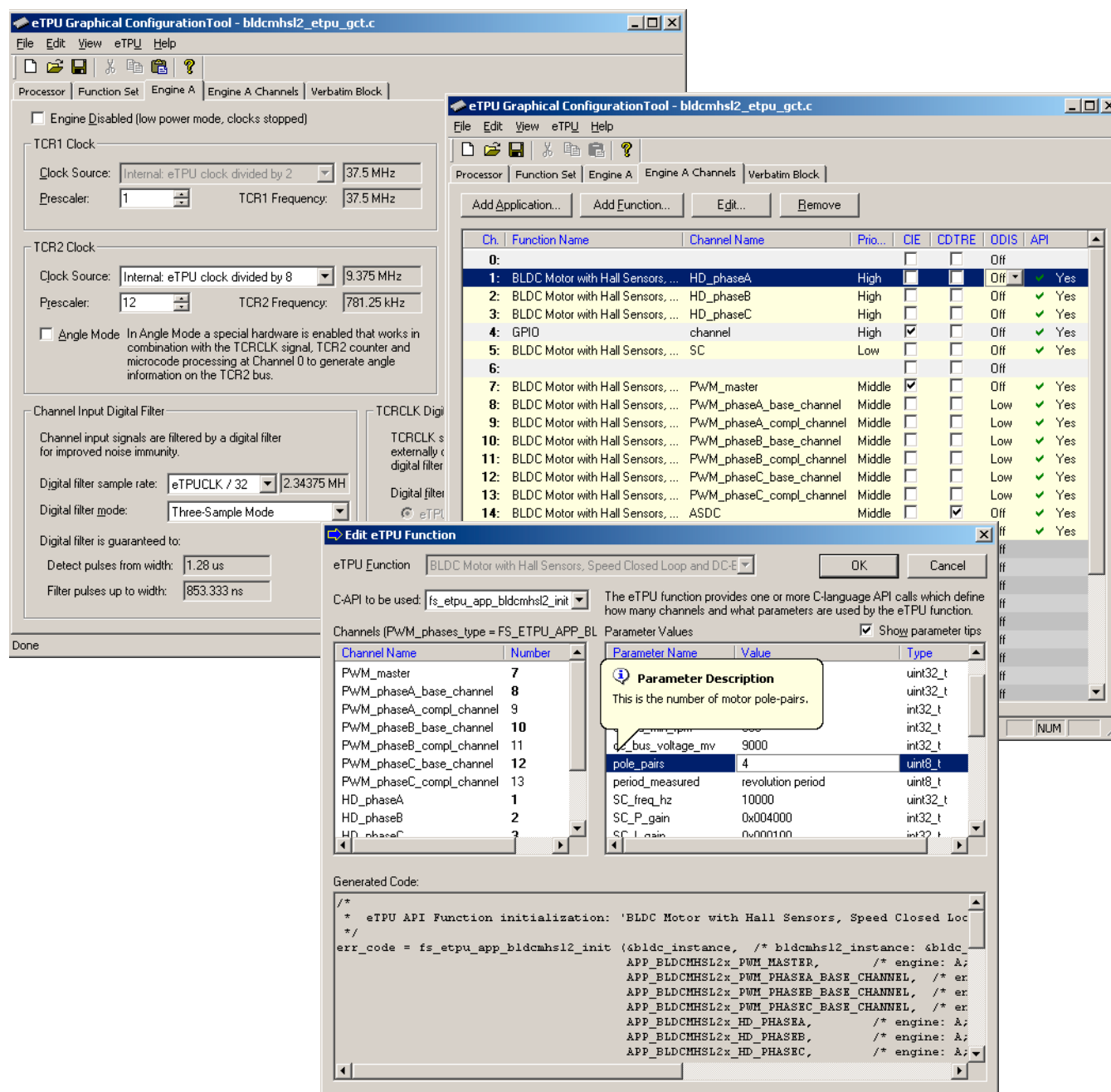
Channel 3 - Hall decoder (HD) - Phase C
 Channel 5 - speed controller (SC)
 Channel 7 - PWM master for DC motors (PWMMDC)
 Channel 8 - PWM commuted (PWMC) - Phase A - base channel
 Channel 10 - PWM commuted (PWMC) - Phase B - base channel
 Channel 12 - PWM commuted (PWMC) - Phase C - base channel
 Channel 14 - Analog sensing for DC motors (ASDC)
 Channel 15 - break controller (BC)

These eTPU channels are initialized by the `fs_etpu_app_bldcmhs12_init` eTPU application API function (see 4.3). The application settings are as follows:

- PWM phases-type is commuted complementary pairs
- PWM frequency 20kHz
- PWM dead-time 1 μ s
- Motor speed range 14 000 RPM
- Motor speed minimum 300 RPM
- DC-bus voltage 9V
- Number of motor pole pairs 4
- Motor speed calculated using HD revolution period
- Speed controller update frequency 10kHz
- PI controller parameters:
 P-gain is 0.5 ($0x004000 * 2^{-15}$), and
 I-gain is 0.0078125 ($0x000100 * 2^{-15}$).
 The controller parameters were experimentally tuned.
- Ramp parameters:
 0.3s to ramp up from zero to the maximum speed,
 0.3s to ramp down from the maximum speed to zero.
- Break controller mode - PWM-based breaking signal is generated in case of over-voltage.
- Break control signal polarity is active high.
- DC-bus voltage level, at which break control signal is ON, is 130% of the nominal DC-bus voltage
- DC-bus voltage level, at which break control signal is OFF, is 110% of the nominal DC-bus voltage
- ASDC function triggers A/D converter on high-low edge
- DC-bus voltage measurement time including A/D conversion time and DMA transfer time is 11 μ s
- `p_ASDC_result_queue` pointer contains the address of the measured sample of DC-bus voltage
- Measured sample of DC-bus voltage is shifted left by 10 bits

- DC-bus voltage sample offset within ASDC_result_queue is 0
- ASDC EWMA filter time constant is 450 us
- Channel 4 - general purpose I/O (GPIO)
 - This eTPU channel is initialized by the `fs_etpu_gpio_init` API function. The setting is:
 - channel priority: high

The `my_system_etpu_start` function first applies the settings for the channel interrupt enable and channel output disable options, then enables the eTPU timers, so starting the eTPU.



4.2.1.2 Initialization of FreeMASTER Communication

Prior to the FreeMASTER initialization, it is necessary to set pointers to the eTPU functions DATA RAM bases and configuration register bases. Based on these pointers, which are read by FreeMASTER during the initialization, the locations of all eTPU function parameters and configuration registers are defined. This is essential for correct FreeMASTER operation!

FreeMASTER consists of software running on a PC and on the microprocessor, connected via an RS-232 serial port. A small program resident in the microprocessor communicates with the FreeMASTER on the PC in order to return status information to the PC, and processes control information from the PC. The microprocessor part of the FreeMASTER is initialized by two functions: `iniFmasterUart` and `fmasterInit`. Both functions are included in `fmaster.c`, which automatically initializes the UART driver and installs all necessary services.

4.2.1.3 Initialization of needful peripheral modules

Several peripheral modules needed for DC-bus voltage measurement processing must be initialized:

- An external analog to digital converter AD7928BRA, interfaced to the CPU via the QSPI, is used for sampling the DC-bus voltage analog value. Initialization of the AD Converter and QSPI module is done by the `ADCInit` routine.
- 4 DMA channels and a DMA Timer are used to periodically transfer data from QSPI to the eTPU data memory. Initialization of these modules is done by the `DMAInit` routine.

For a detailed description of DC-bus voltage measurement and data transfer processing, see [4.4.5](#)

4.2.2 APP_STATE_STOP

In this state, the PWM signals are disabled and the motor is off. The motor shaft can be rotated by hand, which enables the user to explore the functionality of the Hall decoder (HD) eTPU function, to watch variables produced by the HD, and to see Hall sensor signals in FreeMASTER.

When the ON/OFF switch is turned on, the application goes through `APP_STATE_ENABLE` to `APP_STATE_RUN`.

4.2.3 APP_STATE_ENABLE

This state is passed through only. The following actions are performed in order to switch the motor drive on:

- Reset the required speed
- Enable the generation of PWM signals

If the PWM phases were successfully enabled, the GPIO eTPU function is configured as input, interrupt on rising edge, and `APP_STATE_RUN` is entered. Where the PWM phases were not successfully enabled, the application state does not change.

4.2.4 APP_STATE_RUN

In this state, the PWM signals are enabled and the motor is on. The required motor speed can be set using the up and down buttons on the M523xEVB or by using FreeMASTER. The latest value is periodically written to the eTPU.

When the ON/OFF switch is turned off, the application goes through APP_STATE_DISABLE to APP_STATE_STOP.

4.2.5 APP_STATE_DISABLE

This state is passed through only. The following actions are performed in order to switch the motor drive off:

- Reset the required speed
- Disable the generation of PWM signals

If PWM phases were successfully disabled, APP_STATE_STOP is entered. Where PWM phases were not successfully disabled, the application state remains the same.

4.2.6 APP_STATE_MOTOR_FAULT

This state is entered after the over-current fault interrupt service routine. The application waits until the ON/OFF switch is turned off. This clears the fault and the application enters the APP_STATE_STOP.

4.2.7 APP_STATE_GLOBAL_FAULT

This state is entered after the eTPU global exception interrupt service routine. The application waits until the ON/OFF switch is turned off. This clears the fault and the application enters the APP_STATE_INIT.

4.3 eTPU Application API

The eTPU application API encapsulates several eTPU function APIs. The eTPU application API includes CPU methods which enable initialization, control, and monitoring of an eTPU application. The use of eTPU application API functions eliminates the need to initialize and set each eTPU function separately, and ensures correct cooperation of the eTPU functions. The eTPU application API is device independent and handles only the eTPU tasks.

In order to shorten the eTPU application names, abbreviated application names are introduced. The abbreviations include the following:

- Motor type (DCM = DC motor, BLDCM = brushless DC motor, PMSM = permanent magnet synchronous motor, ACIM = AC induction motor, SRM = switched reluctance motor, SM = stepper motor)
- Sensor type (H = hall sensors, E = shaft encoder, R = resolver, S = sincos, X = sensorless)
- Control type (OL = open loop, PL = position loop, SL = speed loop, CL = current loop, SVC = speed vector control, TVC = torque vector control)

Based on these definitions, the BLDCMHSL2 is an abbreviation for BLDC motor with hall sensors and speed closed loop eTPU motor - control application. As there are several BLDC motor applications with hall sensors and speed closed loop, the number 2 denotes the second such application in order. This second application, moreover, demonstrates the break controller eTPU function usage for DC-bus over-voltage protection.

The BLDCMHSL2 eTPU application API is described in the following paragraphs. There are 5 basic functions added to the BLDCMHSL2 application API. The routines can be found in the `etpu_app_bldcmhsl2.c/.h` files. All BLDCMHSL2 application API routines will be described in order and are listed below:

- Initialization function:

```
int32_t fs_etpu_app_bldcmhsl2_init(
    bldcmhsl2_instance_t * bldcmhsl2_instance,
        uint8_t    PWM_master_channel,
        uint8_t    PWM_phaseA_channel,
        uint8_t    PWM_phaseB_channel,
        uint8_t    PWM_phaseC_channel,
        uint8_t    HD_phaseA_channel,
        uint8_t    HD_phaseB_channel,
        uint8_t    HD_phaseC_channel,
        uint8_t    SC_channel,
        uint8_t    BC_channel,
        uint8_t    ASDC_channel,
        uint8_t    PWM_phases_type,
        uint32_t    PWM_freq_hz,
        uint32_t    PWM_dead_time_ns,
        int32_t     speed_range_rpm,
        int32_t     speed_min_rpm,
        int32_t     dc_bus_voltage_mv,
        uint8_t     pole_pairs,
        uint8_t     period_measured,
        uint32_t    SC_freq_hz,
        int32_t     SC_P_gain,
        int32_t     SC_I_gain,
        uint32_t    SC_ramp_time_ms,
        uint8_t     BC_mode,
        uint8_t     BC_polarity,
        uint8_t     BC_u_dc_bus_ON_perc,
        uint8_t     BC_u_dc_bus_OFF_perc,
        uint8_t     ASDC_polarity,
        uint24_t    ASDC_measure_time_us,
        uint32_t    *ASDC_result_queue,
        uint8_t     ASDC_bit_shift,
```

```
uint8_t    ASDC_queue_offset,
uint32_t    ASDC_filter_time_constant_us)
```

- Change operation functions:

```
int32_t fs_etpu_app_bldcmhsl2_enable(
    bldcmhsl2_instance_t * bldcmhsl2_instance,
    uint8_t    configuration)
```

```
int32_t fs_etpu_app_bldcmhsl2_disable(
    bldcmhsl2_instance_t * bldcmhsl2_instance)
```

```
fs_etpu_app_bldcmhsl2_set_speed_required(
    bldcmhsl2_instance_t * bldcmhsl2_instance,
    int32_t    speed_required_rpm)
```

- Value return functions:

```
fs_etpu_app_bldcmhsl2_get_data(
    bldcmhsl2_instance_t * bldcmhsl2_instance,
    bldcmhsl2_data_t * bldcmhsl2_data)
```

4.3.1 int32_t fs_etpu_app_bldcmhsl2_init(...)

This routine is used to initialize the eTPU channels for the “BLDC Motor with Speed Closed Loop and DC-Bus Break Controller” application. This function has the following parameters:

- **bldcmhsl2_instance (bldcmhsl2_instance_t*)** - This is a pointer to bldcmhsl2_instance_t structure, which is filled by fs_etpu_app_bldcmhsl2_init. This structure must be declared in the user application. Where there are more instances of the application running simultaneously, there must be a separate bldcmhsl2_instance_t structure for each one.
- **PWM_master_channel (uint8_t)** - This is the PWM master channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.
- **PWM_phaseA_channel (uint8_t)** - This is the PWM phase A channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B. In the case of complementary signal generation (PWM_phases_type==FS_ETPU_APP_BLDCMHSL2_COMPL_PAIRS), the complementary channel is one channel higher.
- **PWM_phaseB_channel (uint8_t)** - This is the PWM phase B channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B. In the case of complementary signal generation (PWM_phases_type==FS_ETPU_APP_BLDCMHSL2_COMPL_PAIRS), the complementary channel is one channel higher.
- **PWM_phaseC_channel (uint8_t)** - This is the PWM phase C channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B. In the case of complementary signal generation (PWM_phases_type==FS_ETPU_APP_BLDCMHSL2_COMPL_PAIRS), the complementary channel is one channel higher.
- **HD_phaseA_channel (uint8_t)** - This is the Hall decoder phase A channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.

- **HD_phaseB_channel (uint8_t)** - This is the Hall decoder phase B channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.
- **HD_phaseC_channel (uint8_t)** - This is the Hall decoder phase C channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.
- **SC_channel (uint8_t)** - This is the speed controller channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.
- **BC_channel (uint8_t)** - This is the break controller channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.
- **ASDC_channel (uint8_t)** - This is the analog sensing for DC motors (ASDC) channel number. 0-31 for ETPU_A, and 64-95 for ETPU_B.
- **PWM_phases_type (uint8_t)** - This parameter determines the type of all PWM phases. This parameter should be assigned a value of:
FS_ETPU_APP_BLDCMHSL2_SINGLE_CHANNELS, or
FS_ETPU_APP_BLDCMHSL2_COMPL_PAIRS.
- **PWM_freq_hz (uint32_t)** - This is the PWM frequency in Hz.
- **PWM_dead_time_ns (uint32_t)** - This is the PWM dead-time in ns.
- **speed_range_rpm (int32_t)** - This is the maximum motor speed in rpm.
- **speed_min_rpm (int32_t)** - This is the minimum (measurable) motor speed in rpm.
- **dc_bus_voltage_mv (int32_t)** - This is the DC-bus voltage in mV.
- **pole_pairs (uint8_t)** - This is the number of motor pole-pairs.
- **period_measured (uint8_t)** - This option defines the type of period measurement for speed calculation. This parameter should be assigned a value of:
FS_ETPU_APP_BLDCMHSL2_REV_PERIOD, or
FS_ETPU_APP_BLDCMHSL2_SECTOR_PERIOD.
- **SC_freq_hz (uint32_t)** - This is the speed controller update frequency in Hz. The assigned value must be equal to the PWM_freq_hz divided by 1, 2, 3, 4, 5, ...
- **SC_P_gain (fract24_t)** - This is the speed controller P-gain in 24-bit signed fractional format (9.15).
0x008000 corresponds to 1.0
0x000001 corresponds to $0.0000305 (30.5 \times 10^{-6})$
0x7FFFFFFF corresponds to 255.9999695
- **SC_I_gain (fract24_t)** - This is the speed controller I-gain in 24-bit signed fractional format (9.15).
0x008000 corresponds to 1.0
0x000001 corresponds to $0.0000305 (30.5 \times 10^{-6})$
0x7FFFFFFF corresponds to 255.9999695
- **SC_ramp_time_ms (uint32_t)** - This parameter defines the required speed ramp time in ms. A step change of the required speed from 0 to speed_range_rpm is slowed down by the ramp to take the defined time.

- **BC_mode (uint8_t)** - This is the function mode. This parameter should be assigned a value of: FS_ETPU_APP_BLDCMHSL2_BC_MODE_ON_OFF, or FS_ETPU_APP_BLDCMHSL2_BC_MODE_PWM.
- **BC_polarity (uint8_t)** - This is the BC output polarity. This parameter should be assigned a value of: FS_ETPU_APP_BLDCMHSL2_BC_ON_HIGH, or FS_ETPU_APP_BLDCMHSL2_BC_ON_LOW.
- **BC_u_dc_bus_ON_perc (uint8_t)** - This is the proportion between U_DC_BUS, above which the BC output is ON, and the nominal U_DC_BUS, expressed in percentage (usually about 130%).
- **BC_u_dc_bus_OFF_perc (uint8_t)** - This is the proportion between U_DC_BUS, below which the BC output is OFF, and the nominal U_DC_BUS, expressed in percentage (usually about 110%).
- **ASDC_polarity (uint8_t)** - This is the polarity to assign to the ASDC function. This parameter should be assigned a value of: FS_ETPU_APP_BLDCMHSL2_ASDC_PULSE_HIGH or FS_ETPU_APP_BLDCMHSL2_ASDC_PULSE_LOW.
- **ASDC_measure_time_us (uint24_t)** - Time from the first (triggering) edge to the second edge, at which the result queue is supposed to be ready in the DATA_RAM (in us). This value depends on the A/D conversion time and DMA transfer time.
- **ASDC_result_queue (uint32_t *)** - Pointer to the result queue. Result queue is an array of 16-bit words that contains the measured values.
- **ASDC_bit_shift (uint8_t)** - This parameter defines how to align data from the result queue into fract24 (or int24). This parameter should be assigned a values of: FS_ETPU_APP_BLDCMHSL2_ASDC_SHIFT_LEFT_BY_8, FS_ETPU_APP_BLDCMHSL2_ASDC_SHIFT_LEFT_BY_10, FS_ETPU_APP_BLDCMHSL2_ASDC_SHIFT_LEFT_BY_12, or FS_ETPU_APP_BLDCMHSL2_ASDC_SHIFT_LEFT_BY_16.
- **ASDC_queue_offset (uint8_t)** - Position of the U_DC_BUS sample in the result queue. Offset is defined in bytes.
- **ASDC_filter_time_constant_us (uint32_t)** - This the time constant of the filter which applies when processing the U_DC_BUS samples, in us.

4.3.2 int32_t fs_etpu_app_bldcmhsl2_enable(...)

This routine is used to enable the generation of PWM signals, commutations on Hall signal transitions, and to start the speed controller. This function has the following parameters:

- **bldcmhsl2_instance (bldcmhsl2_instance_t*)** - This is a pointer to bldcmhsl2_instance_t structure, which is filled by fs_etpu_app_bldcmhsl2_init.
- **configuration (uint8_t)** - This is the required configuration of the SC. This parameter should be assigned a value of: FS_ETPU_APP_BLDCMHSL2_SPEED_LOOP_OPENED, or FS_ETPU_APP_BLDCMHSL2_SPEED_LOOP_CLOSED.

4.3.3 int32_t

fs_etpu_app_bldcmhsl2_disable(bldcmhsl2_instance_t * bldcmhsl2_instance)

This routine is used to disable the generation of PWM signals, commutation on Hall signal transitions, and to stop the speed controller. This function has the following parameter:

- **bldcmhsl2_instance (bldcmhsl2_instance_t*)** - This is a pointer to bldcmhsl2_instance_t structure, which is filled by fs_etpu_app_bldcmhsl2_init.

4.3.4 fs_etpu_app_bldcmhsl2_set_speed_required(...)

This routine is used to set the required motor speed. This function has the following parameters:

- **bldcmhsl2_instance (bldcmhsl2_instance_t*)** - This is a pointer to bldcmhsl2_instance_t structure, which is filled by fs_etpu_app_bldcmhsl2_init.
- **speed_required_rpm (int32_t)** - This is the required motor speed in rpm.

4.3.5 fs_etpu_app_bldcmhsl2_get_data(...)

This routine is used to get the application state data. This function has the following parameters:

- **bldcmhsl2_instance (bldcmhsl2_instance_t*)** - This is a pointer to bldcmhsl2_instance_t structure, which is filled by fs_etpu_app_bldcmhsl2_init.
- **bldcmhsl2_data (bldcmhsl2_data_t*)** - This is a pointer to bldcmhsl2_data_t structure of application state data, which is updated.

4.4 eTPU Block Diagram

The eTPU functions used to drive the BLDC motor with speed closed loop and DC-bus break controller are located in the motor-control set of eTPU functions (set3 - DC motors). The eTPU functions within the set serve as building blocks for various motor-control applications. The following paragraphs describe the functionality of each block.

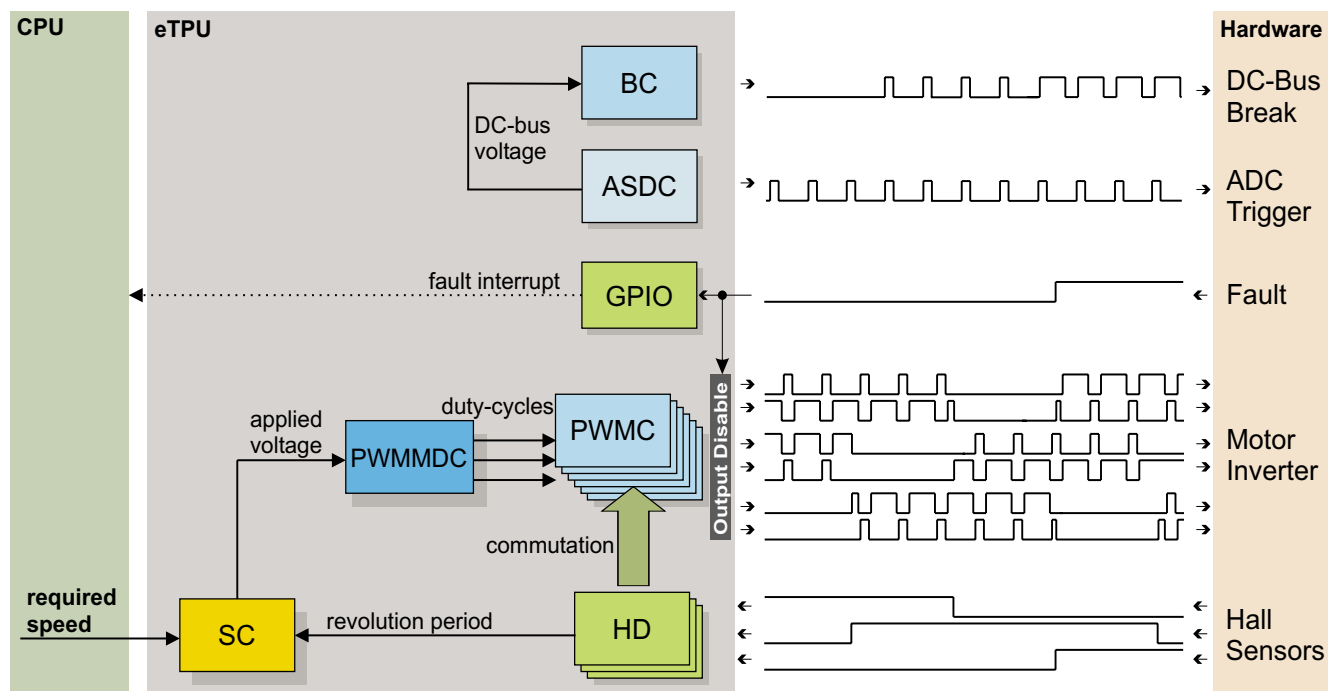


Figure 21. Block Diagram of eTPU Processing

4.4.1 PWM Generator (PWMMDC+PWMC)

The generation of PWM signals for motor-control applications with eTPU is provided by three eTPU functions:

- PWM - master for DC motors (PWMMDC)
- PWM - full range (PWF)
- PWM - commuted (PWMC)

The PWM master for DC motors (PWMMDC) function calculates a PWM duty cycle and updates the three PWM phases. The phases may be driven either by the PWM full range (PWF) function, which enables a full (0% to 100%) duty-cycle range, or by the PWM commuted (PWMC) function, which enables switching the phase ON and OFF. The PWMC function is used in the described application.

The PWMC function generates the PWM signals. The PWMMDC function controls three PWMC functions, three PWM phases, and does not generate any drive signal. The PWMMDC can be executed even on an eTPU channel not connected to an output pin (channels 16 to 32).

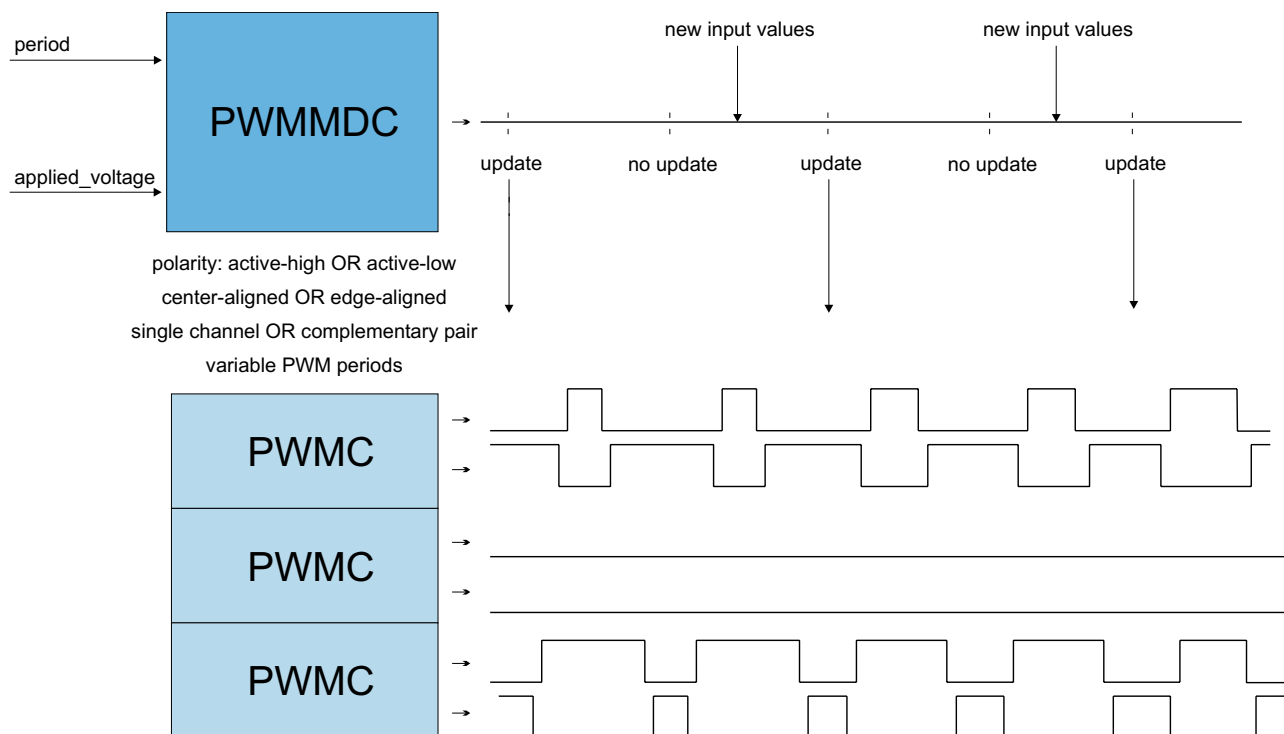


Figure 22. Functionality of PWMMDC+PwMC

For more details about the PWMMDC, PWMF, and PwMC eTPU functions, refer to Reference 9.

4.4.2 Hall Decoder (HD)

The Hall decoder eTPU function is intended to process signals generated by Hall sensors in motion control systems. The HD function uses three adjacent eTPU channels configured as inputs. The HD function calculates the following parameters for the CPU:

- Sector - determines the position of the motion system in one of the sectors.
- Direction - determines the direction of the motion system. A direction value 0 means a positive (incremental) direction, other values mean a negative (decremental) direction.
- Revolution counter - determines the number of motion system electrical revolutions. The revolution counter is incremented or decremented on each revolution, based on the current direction.
- Revolution period - determines the TCR time of the last revolution. The parameter value is updated each time the sector is changed. The revolution period is measured from the last edge of a similar type (low-high / high-low), on the same channel, to the current edge.
- Sector period - determines the TCR time between the last two changes of the sector. The parameter value is updated each time the sector is changed. The sector period is measured from the last edge to the current edge.
- Last edge time - stores the tcR time of the last incoming edge.

The HD function also performs commutations of PwMC phases.

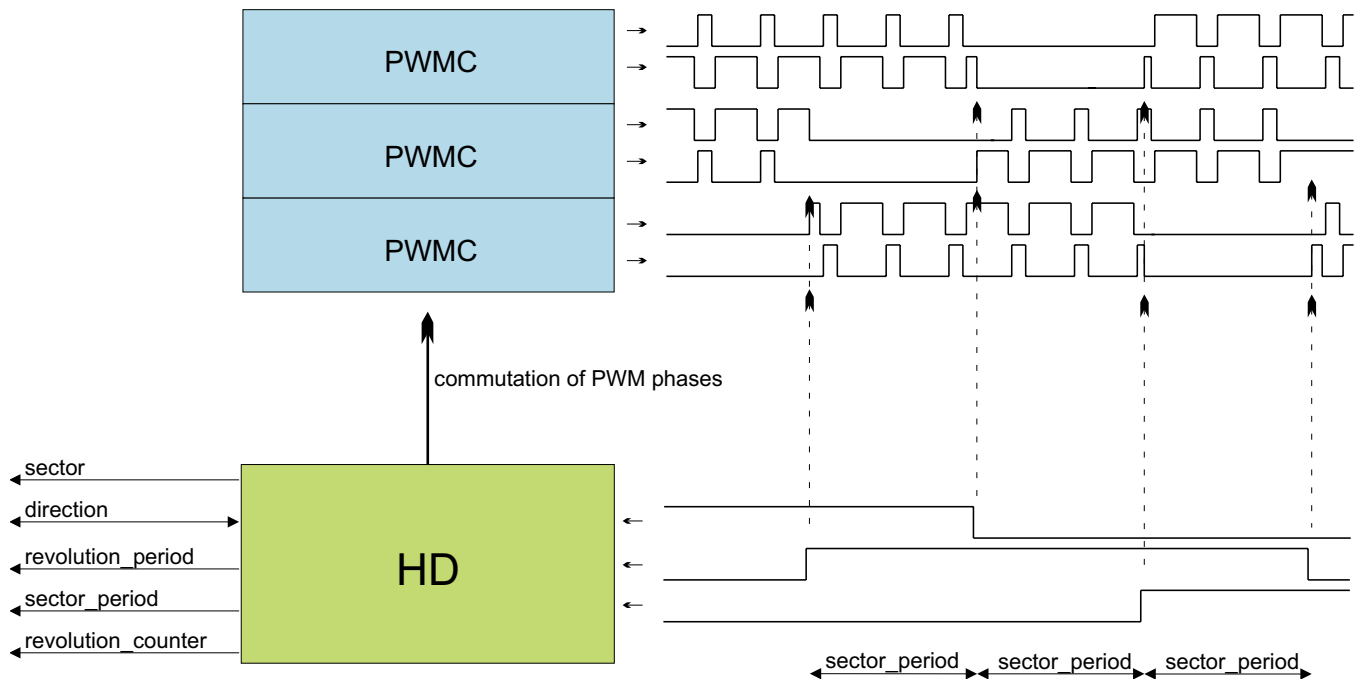


Figure 23. Functionality of HD

For more details about the HD eTPU function, refer to Reference [7](#).

4.4.3 Speed Controller (SC)

The speed controller eTPU function is not intended to process input or output signals. Its purpose is to control another eTPU function’s input parameter. The SC function can be executed even on an eTPU channel not connected to an output pin. The SC function includes a general PID controller algorithm. The controller calculates its output based on two inputs: a measured value and a required value. The measured value (the actual motor speed) is calculated based on inputs provided by the HD function. The required value is an output of the speed ramp, whose input is a SC function parameter and can be provided by the CPU or another eTPU function. In the motor-control eTPU function set, this function mostly provides the speed outer-loop.

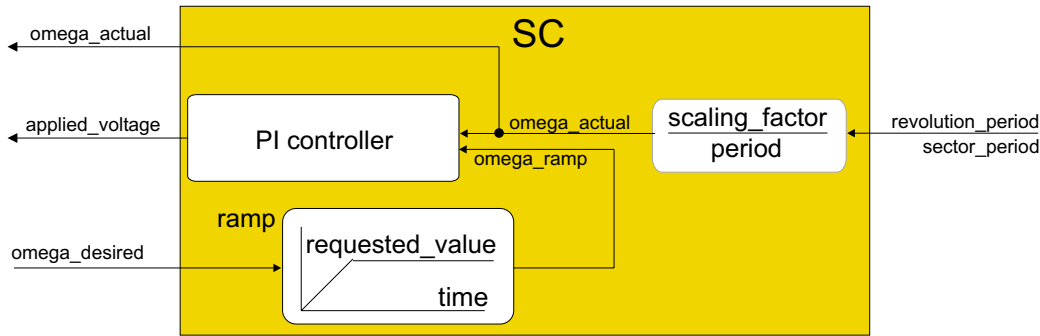


Figure 24. Functionality of SC

4.4.4 Break Controller (BC)

The purpose of the break controller (BC) eTPU function is to eliminate DC-bus overvoltage when a motor is driven in the generating mode. The BC function generates the DC-bus break control signal (see Figure 25) based on the actual DC-bus voltage.

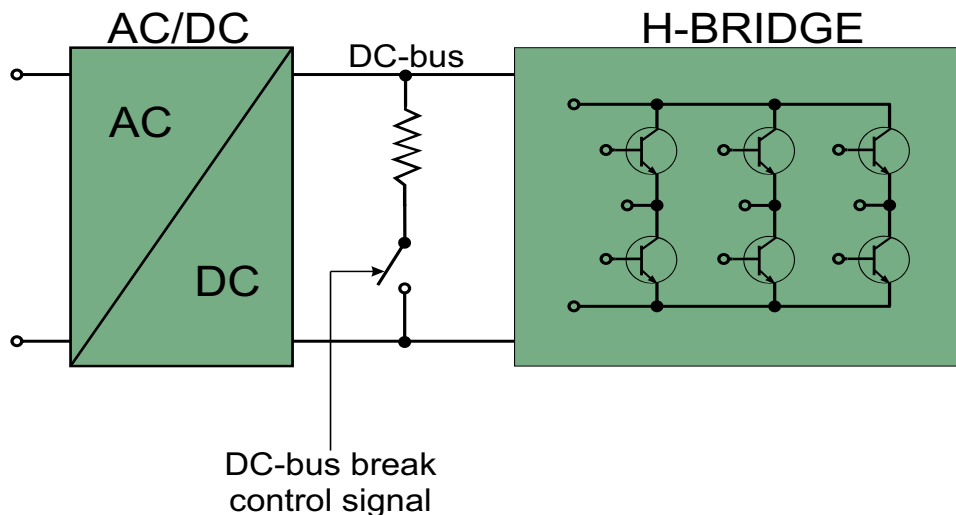


Figure 25. Functionality of BC

The described application uses the PWM mode of the BC function. In this mode, the BC function switches softly using a PWM signal. The $u_dc_bus_ON$ and $u_dc_bus_OFF$ thresholds define a ramp (see Figure 26). When the DC-bus voltage is lower than $u_dc_bus_OFF$, the control signal is turned off. Between the $u_dc_bus_OFF$ and $u_dc_bus_ON$ thresholds, a PWM signal with a duty-cycle linearly increasing from 0% to 100% is generated. Above the $u_dc_bus_ON$ threshold, the control signal is turned on. The functionality of the BC is shown in figures 27, 28, 29. Signal 1 (dark blue line) represents the DC-bus voltage, signal 2 (light blue line) reflects the DC-bus break control signal generated by the BC.

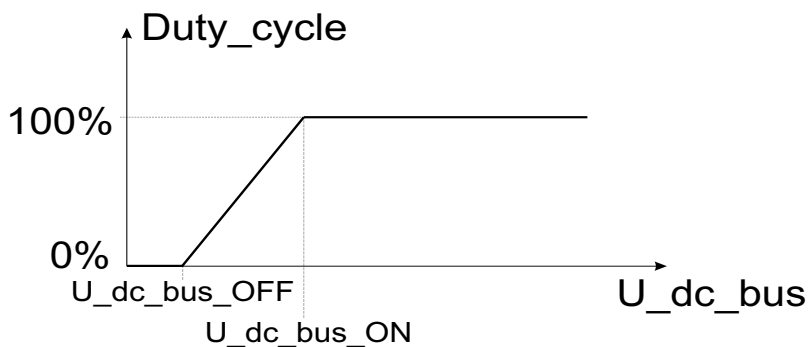


Figure 26. PWM Mode of the Break Controller Function

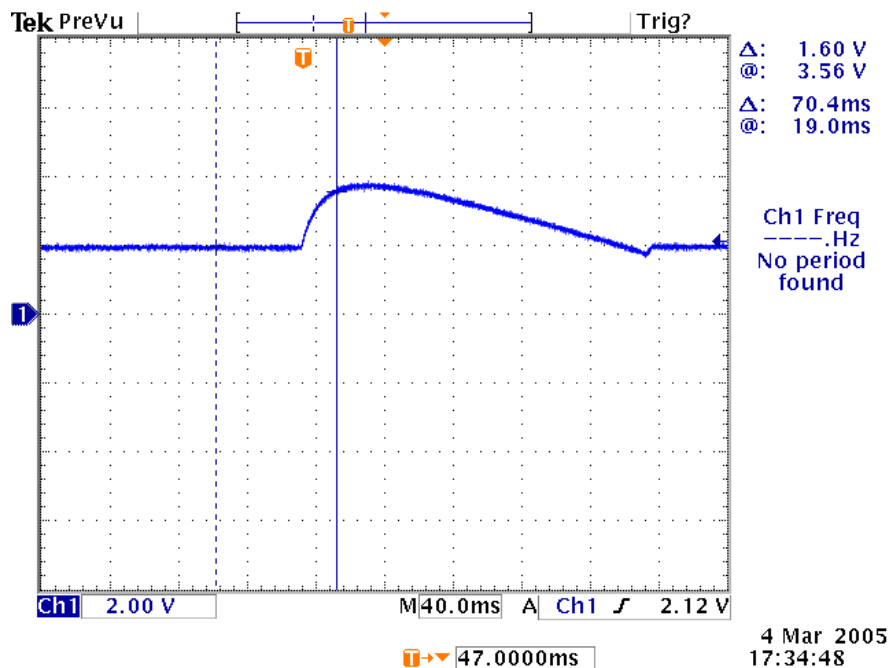


Figure 27. Oscilloscope Screen-shot Showing DC-bus Voltage Course when a Motor Reaches to Generating Mode (Without Action of Break Controller)

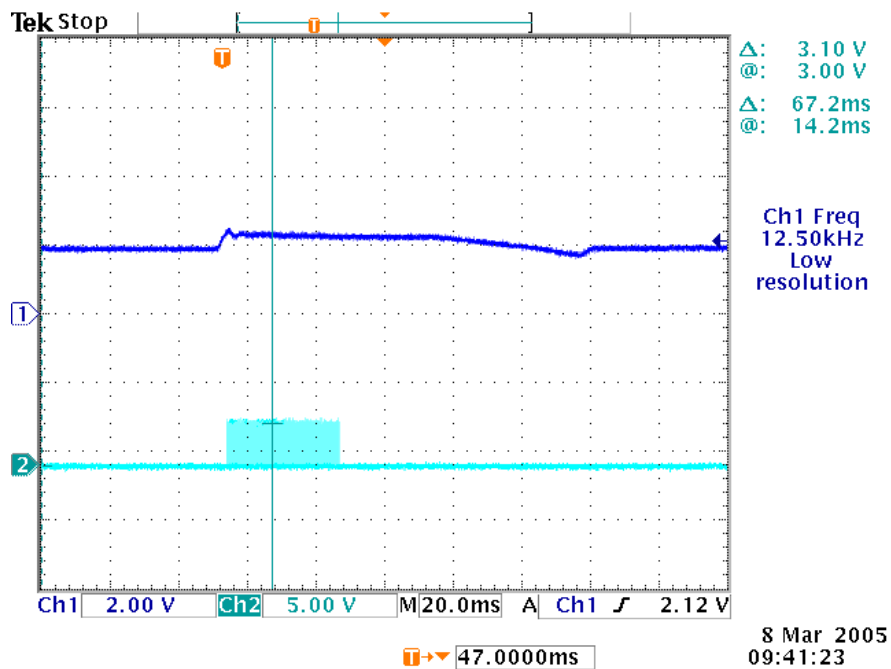


Figure 28. Oscilloscope Screen-shot Showing Functionality of the Break Controller

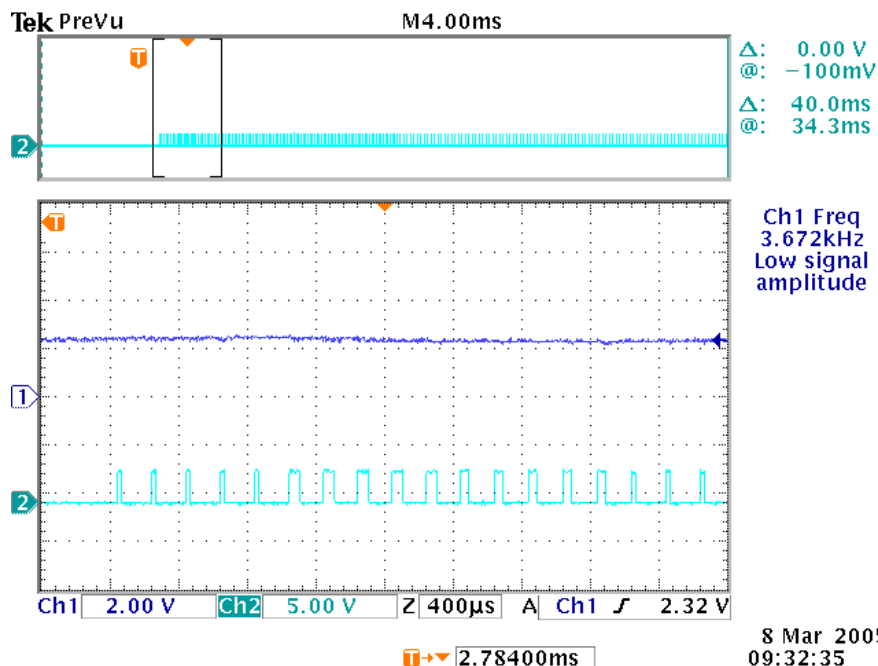


Figure 29. Oscilloscope Screen-shot showing Functionality of the Break Controller in Detail (Zoom of DC-bus Break Control Signal)

For more details about the BC eTPU function, refer to Reference 10.

4.4.5 Analog Sensing for DC Motors (ASDC)

The analog sensing for DC motors eTPU function (ASDC) is useful for preprocessing analog values that are measured by the AD converter and transferred to the eTPU data memory by DMA transfer. The ASDC function is also useful for triggering the AD converter and synchronizing other eTPU functions.

All the above mentioned ASDC features are utilized in the application. The ASDC is initialized to run in PWM synchronized mode, e.g. the first ASDC edge is synchronized with the beginning of the PWM period. Simultaneously, the ASDC manages to synchronize the BC function by generating the link to the BC channel every 16th ASDC period.

The ASDC function preprocesses the DC-bus voltage analog value and passes the adjusted value as an input to the BC function. Processing of the DC-bus voltage analog value includes bit shifting and filtering.

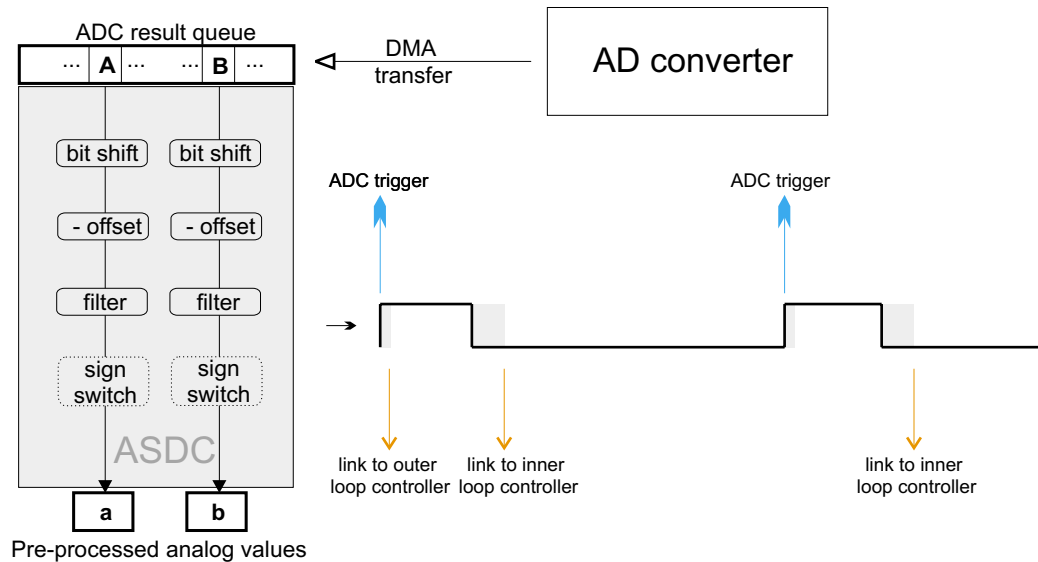


Figure 30. Functionality of ASDC

In order to ensure periodic sampling of the DC-bus voltage and the quick transfer of the measured data from the AD converter to the ETPU DATA RAM, several peripheral modules are used (see [Figure 31](#)):

- An external analog to digital converter (AD7928BRA) is used for sampling of the DC-bus voltage analog value.
- A queued serial peripheral interface (QSPI) module is used to interface the AD converter. It enables initialization of the AD converter control registers, triggering the AD converter, and receiving measured samples of DC-bus voltage.
- Direct memory access timer 0 (DMA timer 0) is used for the DMA request assertion at the time the measured sample is ready in the QSPI receive RAM. DMA timer 0 is configured to run in reference compare mode, asserting the DMA request a defined time after the AD converter triggering. This sampling time is defined in the DTRR0 register of the DMA timer.
- 4 direct memory access (DMA) channels are used as follows:
 - DMA channel 3 is used for the transfer of one auxiliary byte (0x80) from the ETPU DATA RAM to the QDLYR register of the QSPI module. This operation triggers the QSPI transfer and the consequent AD converter sampling. The DMA channel 3 transfer is initiated by the DMA request generated by the ASDC eTPU function. When the transfer is complete, the link to DMA channel 1 is made causing the DMA request assertion on DMA channel 1.
 - DMA channel 1 is used for the transfer of one auxiliary byte (0x80) from the ETPU DATA RAM to the DTCN0 register of DMA timer 0 module. This operation clears the DTCN0 register and thus triggers the DMA timer 0 free-running timer counting. The DMA channel 1 transfer is initiated by the link from DMA channel 3.
 - DMA channel 0 is used for the transfer of the measured sample (2 bytes) from the QDR register of the QSPI module to the ETPU DATA RAM. The DMA channel 0 transfer is initiated by a DMA request generated by DMA timer 0, at the time the counter value reaches the reference value. When the transfer is complete, the link to DMA channel 2 is made,

causing the DMA request assertion on DMA channel 2.

- DMA channel 2 is used for the transfer of one auxiliary byte (0x10) from the ETPU DATA RAM to the QAR register of the QSPI module. This operation sets the pointer in the QSPI to the start of the receive RAM, thus enabling the same sample to be reading in the next cycle. The DMA channel 2 transfer is initiated by the link from DMA channel 0.

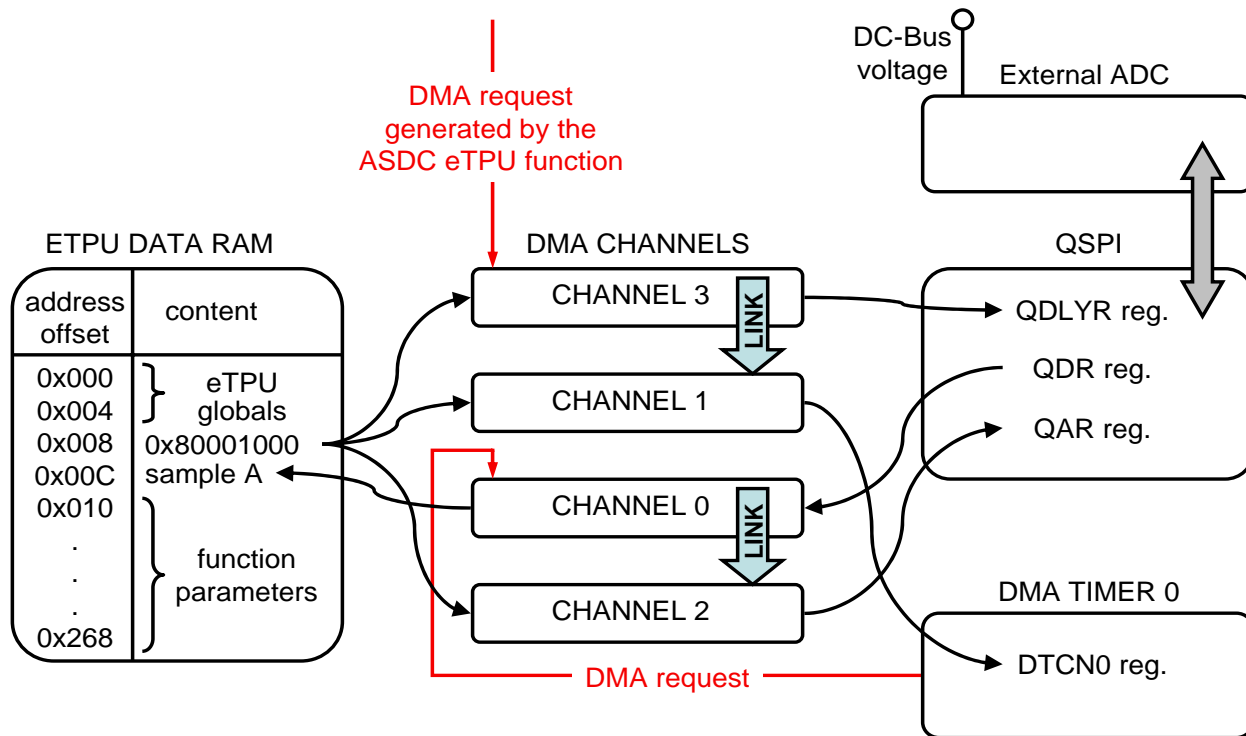


Figure 31. DC-bus Voltage Sample Transfer to the ETPU DATA RAM

As each of the DMA transfers decrements the DMA BCRx registers by one (DMA channels 1, 2, 3), or by two (DMA channel 0), re-initializing all these registers must be done regularly to enable the continuous operation of the DMA channels in this way (see 4.1.2).

4.4.6 General Purpose I/O (GPIO)

This function originates from the general eTPU function set (set1) and is included in the DC motor control eTPU function set as well. It allows the user to configure an eTPU channel as a general purpose input or output. There are 7 function modes supported:

- Input mode - update periodically
- Input mode - update on transition - either edge
- Input mode - update on transition - falling edge
- Input mode - update on transition - rising edge
- Input mode - update on request/disable transition and match updates

- Output mode - output low
- Output mode - output high

GPIO function is configured to generate an interrupt to the CPU in case of an overcurrent fault. The fault signal, which is usually connected to the eTPU output disable input, can be also connected to the eTPU channel assigned a GPIO function. When the fault signal turns active, selected output channels are immediately disabled by the eTPU hardware. At the same time, the GPIO function generates an interrupt, in order to notify the CPU about the fault occurrence.

For more details about the GPIO eTPU function, refer to Reference [12](#).

4.5 eTPU Timing

eTPU processing is event-driven. Once an event service begins, its execution cannot be interrupted by another event service. The other event services have to wait, which causes a service request latency. The maximum service request latency, or worst case latency (WCL), differs for each eTPU channel. The WCL is affected by the channel priority and activity on other channels. The WCL of each channel must be kept below a required limit. For example, the WCL of the PWMC channels must be lower than the PWM period.

A theoretical calculation of WCLs, for a given eTPU configuration, is not a trivial task. The motor control eTPU functions introduce a debugging feature that enables the user to check channel latencies using an oscilloscope, and eliminates the necessity of theoretical WCL calculations.

As mentioned earlier, some eTPU functions are not intended to process any input or output signals for driving the motor. These functions turn the output pin high and low, so that the high-time identifies the period of time in which the function execution is active. An oscilloscope can be used to determine how much the channel activity pulse varies in time, which indicates the channel service latency range. For example, when the oscilloscope time base is synchronized with the PWM periods, the behavior of a tested channel activity pulse can be described by one of the following cases:

- The pulse is asynchronous with the PWM periods. This means that the tested channel activity is not synchronized with the PWM periods.
- The pulse is synchronous with the PWM periods and stable. This means that the tested channel activity is synchronous with the PWM periods and is not delayed by any service latency.
- The pulse is synchronous with the PWM periods but its position varies in time. This means that the tested channel activity is synchronous with the PWM periods and the service latency varies in this time range.

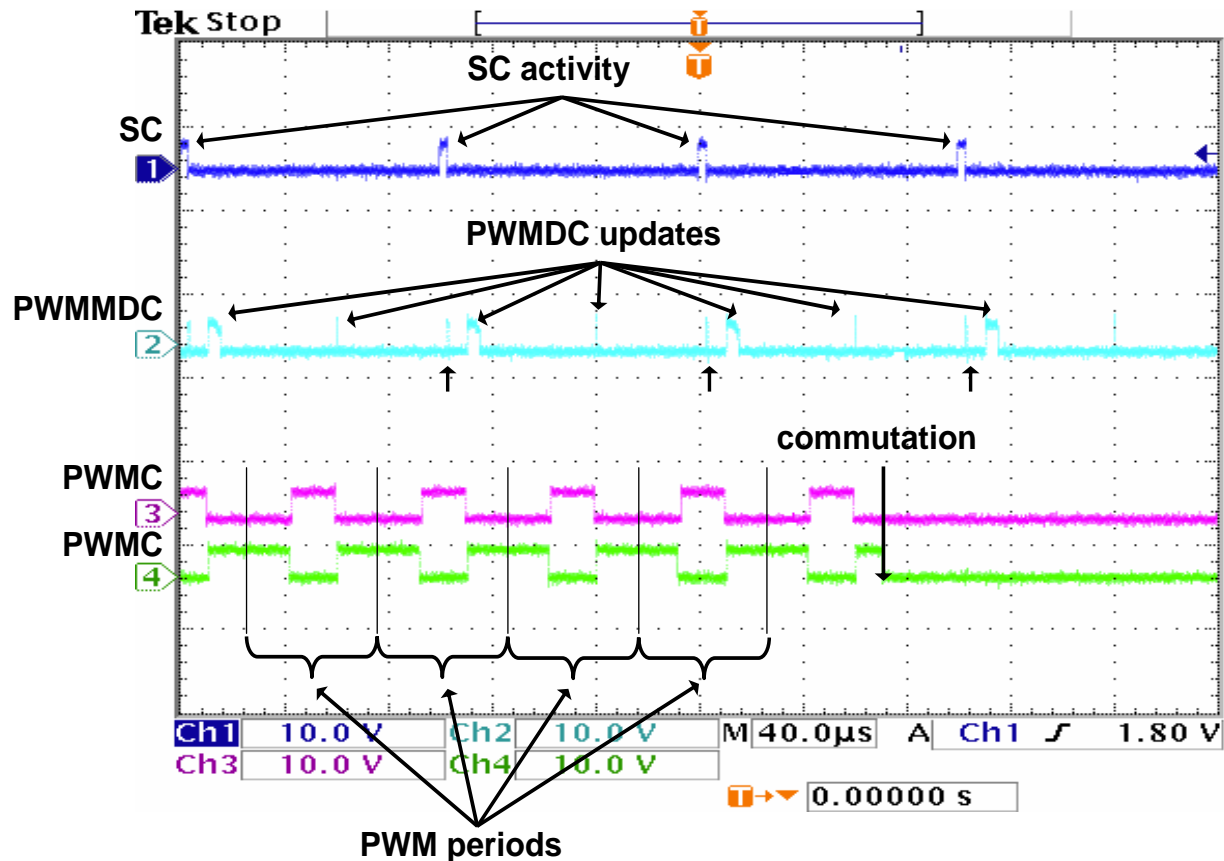


Figure 32. Oscilloscope Screen-shot and Explanation of eTPU Timing

Figure 32 explains the application eTPU timing. The oscilloscope screen-shot depicts a typical situation described below. A live view on the oscilloscope screen enables the user to see the variation of SC and PWMDC activity pulses, which determines the channel service latency ranges.

In Figure 32, signals 3 (pink) and 4 (green) are PWM signals of one phase. It is a complementary pair of center-aligned PWM signals. The base channel (3) is of active-high polarity, while the complementary channel (4) is active-low. The PWM phase commutation is recognizable on the screen. The PWM period is 50μs, which corresponds to a PWM frequency of 20kHz.

Signal 1 (blue) is generated by the speed controller (SC) eTPU function. Its pulses determine the activity of the SC. The pulse width determines the time necessary to calculate the motor speed from a revolution period measured by the Hall decoder (HD), calculate the required speed ramp, and apply the PI controller algorithm. This output is the new value of applied motor voltage. This calculation is performed periodically at a 10kHz rate, which is every second PWM period.

Signal 2 (cyan) is generated by the PWM master for DC motors (PWMDC) eTPU function. Its pulses determine the activity of the PWMDC. Immediately after each SC pulse, a very narrow PWMDC pulse occurs. These pulses determine the service time of an SC request to update the new value of applied motor voltage. Apart from these pulses, for every PWM period, a pulse will appear which signals a PWM update. The PWM update activity pulse is sometimes narrow and sometimes wide. The pulse is wide when

a new value of applied motor voltage has been processed; it is narrow when no new value has been processed and the PWM duty-cycles are not updated.

The live view on the oscilloscope screen shows that the range of the SC and PWMMDC channel service latencies are very low. The only noticeable latency is caused by Hall decoder (HD) activity. The HD eTPU function processes the Hall signals transitions and commutes the PWM phases. The Hall signals transitions come asynchronously with the PWM periods.

The `fs_etpu_pwmmdc_init_3ph` function parameter `update_time` enables the user to adjust the position of the PWMMDC activity pulse relative to the PWM period frame. The activity pulse has a scheduled `update_time` prior to the end of the period frame, so that the update is finished by the end of the period frame, even in the worst case latency. Reference 9 describes how to set the `update_time` value. The difference between the values of the `fs_etpu_pwmmdc_init_3ph` function parameter `start_offset`, and the `fs_etpu_sc_init` function parameter `start_offset`, determines the position of the SC activity pulse relative to the PWM period frame. The SC activity precedes the PWMMDC activity, so that the worst case SC latency does not affect the PWMMDC latency.

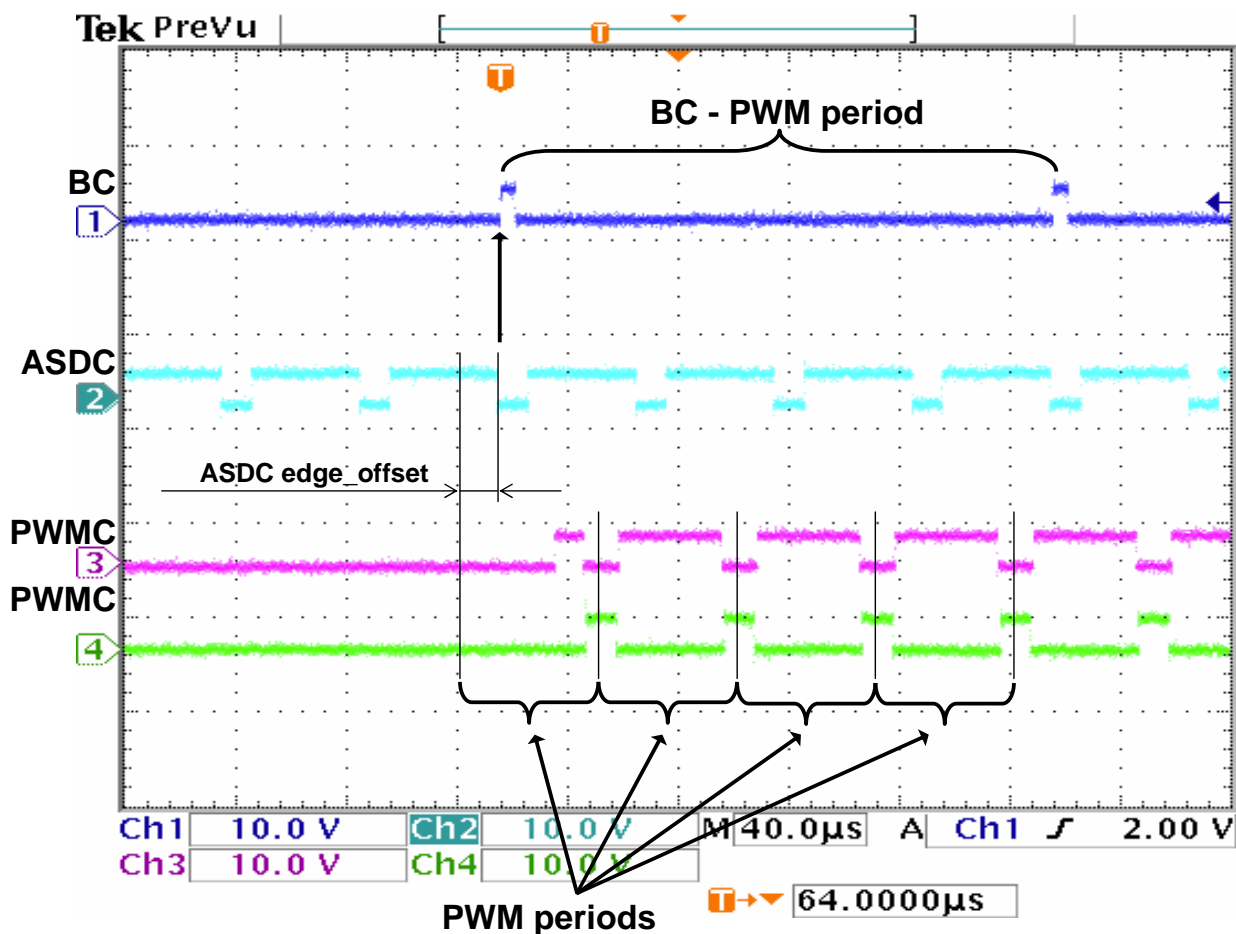


Figure 33. Oscilloscope Screen-shot and Explanation of ASDC and BC Timing

Figure 33 explains the timing of ASDC and BC eTPU functions. Signals 3 (pink) and 4 (green) are PWM signals of one phase, as in Figure 32. Signal 2 (cyan) is generated by the ASDC eTPU function. The ASDC

function triggers the AD converter by generating a DMA request on a high-low edge (active low polarity of ASDC) and simultaneously sending the link to the BC channel every 16th ASDC period (see [Figure 33](#)). The position of the ASDC first edge is synchronized with the beginning of the PWM period. The time between the PWM period beginning and the ASDC first edge equals to one-quarter of the PWM period. The ASDC pulse width determines the time necessary to sample the DC-bus voltage and to transfer this sampled value to the eTPU data memory. ASDC starts measured sample preprocessing at the time of the second edge when a sample is supposed to be ready in the eTPU data memory.

The break controller eTPU function responds to the link generated by the ASDC function every 16th ASDC period. When the break controller channel receives the link, the updated value of DC-bus voltage is compared with the defined over-voltage thresholds, and according to this comparison it generates the PWM-based break control signal - signal 1 (blue) in [Figure 33](#). The period of this signal is 200μs, which corresponds to the frequency of 5kHz.

5 Implementation Notes

5.1 Scaling of Quantities

The BLDC motor control algorithm running on eTPU uses a 24-bit fractional representation for all real quantities except time. The 24-bit signed fractional format is represented using 1.23 format (1 sign bit, 23 fractional bits). The most negative number that can be represented is -1.0, whose internal representation is 0x800000. The most positive number is 0x7FFFFFFF or $1.0 - 2^{-23}$.

The following equation shows the relationship between real and fractional representations:

$$\text{Fractional Value} = \frac{\text{Real Value}}{\text{Real Quantity Range}}$$

where:

Fractional value is a fractional representation of the real value [fract24]

Real value is the real value of the quantity [V, A, RPM, etc.]

Real quantity range is the maximal range of the quantity, defined in the application [V, RPM, etc.]

5.1.1 PI Controller Parameters

The PI controller parameters are set in a 32-bit extended fractional format 9.23. This format enables the user to set values in the range of -256.0 to $256.0 - 2^{-23}$. Internally, the parameter value is transformed into one of two 24-bit formats, either 9.15, or 1.23, based on the value.

5.2 Speed Calculation

The speed controller (SC) eTPU function calculates the angular motor speed using a revolution period measured by the Hall decoder (HD) eTPU function. Optionally, the speed controller can use the sector period instead of the revolution period. The sector period is the time between two consecutive Hall signal transitions. A sum of six sector periods equals one revolution period. At a constant speed, each of the six sector periods may have a slightly different value, caused by an angular error in the Hall sensor positions.

This error affects the PI controller behavior in a negative way. The revolution period is not affected by this error because the period is measured from a particular Hall signal transition to the same transition one revolution later. The revolution period is updated on each transition - six times per period.

The revolution period measured by the HD is the period of one electrical revolution. The electrical revolution is related to the mechanical revolution via the number of motor pole-pairs. The Pittman BLDC motor (N2311) is a 4 pole-pair motor. Hence, the mechanical revolution period is a period of four electrical revolutions.

The speed controller calculates the angular motor speed using the following equation:

$$\text{omega_actual} = \frac{1}{\text{revolution_period}} \cdot \text{scaling_factor}$$

where:

Omega_actual [fract24] is the actual angular speed as a fraction of the maximum speed range
1 is expressed as fractional value 0x7FFFFFFF

Revolution_period [number of TCR ticks] is the period of one electrical revolution

Scaling_factor is pre-calculated using the following equation

$$\text{scaling_factor} = \frac{60 \cdot \text{etpu_tcr_freq}}{\text{omega_max} \cdot \text{pole_pairs}}$$

where:

etpu_tcr_freq [Hz] is a frequency of the internal eTPU timer (TCR1 or TCR2) used

Omega_max [RPM] is a maximal speed range

Pole_pairs is a number of motor pole-pairs

The internal eTPU timer (TCR1 or TCR2) frequency must be set so that the calculation of omega_actual both fits into the 24-bits arithmetic and its resolution is sufficient.

5.3 Definition of Commutation Tables

The PWM phases are commuted on each of the Hall signal transitions. This is internally done by applying two commutation commands that are associated with the particular Hall signal transition. The first command turns a phase off, and the second turns another phase on. Such pairs of commutation commands must be defined for each Hall signal transition, low-high and high-low, on each phase, and for both motor directions. These definitions are located in `etpu_app_bldcmhs12.c` file. Each commutation command is a 32-bit word that consists of the following 8-bit parts.

- Channel number of the PWM phase base channel
- New base channel commutation state. It can be:
 - ON_ACTIVE_HIGH
 - ON_ACTIVE_LOW
 - OFF_LOW
 - OFF_HIGH

Implementation Notes

- New complementary channel commutation state. It can be:
 - ON_ACTIVE_HIGH
 - ON_ACTIVE_LOW
 - OFF_LOW
 - OFF_HIGH
- New phase options:
 - DUTY_POS
 - DUTY_NEG

For a full description of all commutation command options, refer to Reference 9.

Figure 34 depicts the Pittman BLDC motor (N2311) motor timing diagram. The following example describes how to define several of the commutation commands based on this timing diagram:

A Hall signal phase A low-high transition comes at 300 electrical degrees (blue dotted line). The PWM phase B is turned off, with the pin in low state, and phase A on, with active-high polarity on the base channel and active-low polarity on the complementary channel, on this transition. Furthermore, the PWM phase B option is set to not change the calculated duty-cycle value, and the phase A option is set to negate the signed duty-cycle value, which generates a negative voltage. On phase A, this applies immediately, while, on phase B, this will apply 60 degrees later, when the phase is commuted on again. So, the commutation commands associated with the phase A low-high transition in an incremental motor direction are defined, using predefined macros, as follows:

```
phaseA_commut_cmds.lh_i_0 = PWM_phaseB_channel+
                           (FS_ETPU_PWMMDC_OFF_LOW  << 8)+
                           (FS_ETPU_PWMMDC_OFF_LOW  << 16)+
                           (FS_ETPU_PWMMDC_DUTY_POS << 24)

phaseA_commut_cmds.lh_i_1 = PWM_phaseA_channel+
                           (FS_ETPU_PWMMDC_ON_ACTIVE_HIGH << 8)+
                           (FS_ETPU_PWMMDC_ON_ACTIVE_LOW  << 16)+
                           (FS_ETPU_PWMMDC_DUTY_NEG      << 24)
```

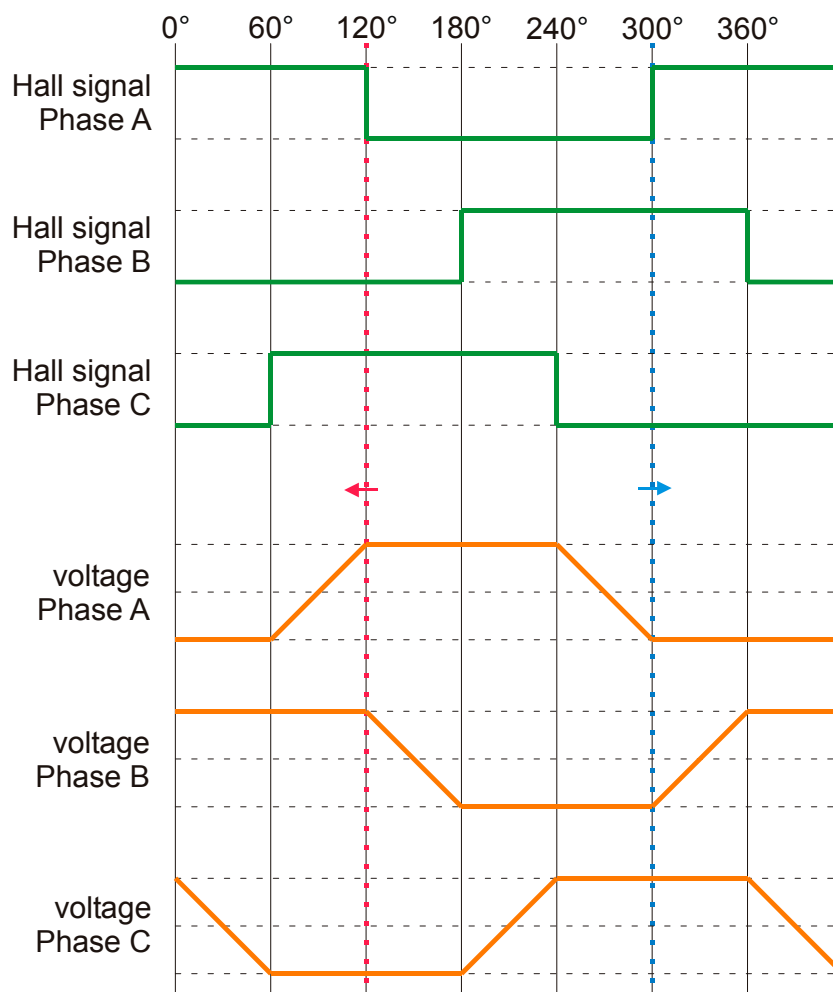


Figure 34. Pittman BLDC Motor (N2311) Timing Diagram

For decremental direction, read the motor timing diagram from right to left. The Hall signal phase A low-high transition comes at 120 electrical degrees (red dotted line). The PWM phase A is turned off and phase B on during this transition. The PWM phase A option is set to negate the duty-cycle in order to generate negative phase voltage, and the phase B option not to negate in order to generate positive voltage. So, the commutation commands associated with the phase A low-high transition in a decremental motor direction are as follows:

```
phaseA_commut_cmds.lh_d_0 = PWM_phaseA_channel+
    (FS_ETPU_PWMMDC_OFF_LOW << 8)+
    (FS_ETPU_PWMMDC_OFF_LOW << 16)+
    (FS_ETPU_PWMMDC_DUTY_NEG << 24)

phaseA_commut_cmds.lh_d_1 = PWM_phaseB_channel+
    (FS_ETPU_PWMMDC_ON_ACTIVE_HIGH << 8)+
    (FS_ETPU_PWMMDC_ON_ACTIVE_LOW << 16)+
```

This way all commutation commands can be defined.

6 Microprocessor Usage

Table 3 shows how much memory is needed to run the application.

Table 3. Memory Usage in Bytes

Memory	Available	Used
FLASH (external)	2M	22256
RAM	6K	1742
eTPU code RAM	6K	4920
eTPU data RAM	1.5K	680

The eTPU module usage in terms of time load can be easily determined based on the following facts:

- According to Reference 9, the maximum eTPU load produced by PWM generation is 946 eTPU cycles per one PWM period. The PWM frequency is set to 20kHz, thus the PWM period is 3750 eTPU cycles (eTPU module clock is 75 MHz, half of the 150 MHz CPU clock).
- According to Reference 8, the speed controller calculation takes 244 eTPU cycles. The calculation is performed every second PWM period.
- According to Reference 7, the processing of one Hall signal transition, including the commutation, takes 308 eTPU cycles. The Hall signal transitions come asynchronously to the PWM periods. Six transitions are processed per one electrical motor revolution.
- According to Reference 11, the ASDC maximum eTPU load takes 42 + 80 eTPU cycles (both the first and then the second edge processing is performed). The ASDC function processing is executed every PWM period.
- According to Reference 10, the BC maximum eTPU load per one update in slave PWM switching mode is 64 eTPU cycles, and the BC maximum eTPU load per one PWM edge is 20 eTPU cycles. The BC update is performed every 16 PWM periods. PWM frequency of the DC-bus break control signal is 5 kHz, which means that the BC-PWM update is performed every 4 PWM periods.
- The GPIO function processing does not affect the eTPU time load.

The values of eTPU load by each of the functions are influenced by compiler efficiency. The above numbers are given for guidance only and are subject to change. For up to date information, refer to the information provided in the latest release available from Freescale.

The peak of the eTPU time load occurs when the speed controller calculation, the break controller update, and a Hall signal transition are processed within one PWM period. This peak value must be kept below 100%, which ensures that all processing fits into the PWM period, no service latency is longer than the PWM period, and thus the generated PWM signals are not affected.

Table 4 shows the eTPU module time load in several typical situations.

Table 4. eTPU Time Load

Situation	Average Time Load [%]	Peak Time Load Within PWM Period [%]
Motor Speed 300 RPM (120 commutations per second)	31.9	45.4
Motor Speed 10000 RPM (4000 commutations per second)	33.5	45.4

7 Summary and Conclusions

This application note provides the user with a description of the demo application BLDC motor with speed closed loop and DC-bus break controller. The application also demonstrates usage of the eTPU module on the ColdFire MCF523x, which results in a CPU independent motor drive. Lastly, the demo application is targeted at the MCF523x family of devices, but it could be easily reused with any device that has an eTPU.

8 References

Table 5. References

1. <i>MCF5235 Reference Manual</i> , MCF5235RM
2. <i>M523xEVB User's Manual</i> , M5235EVBUM
3. <i>33395 Evaluation Motor Board Designer Reference Manual</i> DRM33395/D
4. Pittman's Motors web: http://www.pittmannet.com
5. FreeMASTER web page, http://www.freescale.com , search keyword "FreeMASTER"
6. <i>Enhanced Time Processing Unit Reference Manual</i> , ETPURM
7. "Using the Hall Decoder (HD) eTPU Function," AN2841
8. "Using the Speed Controller (SC) eTPU Function," AN2843
9. "Using the DC Motor Control PWM eTPU Functions," AN2480
10. "Using the Break Controller (BC) eTPU Function," AN2845
11. "Using the Analog Sensing for DC Motors (ASDC) eTPU Function," AN2846

Table 5. References (continued)

12. “Using the General Purpose I/O eTPU functions (GPIO),” AN2850
13. “Using the DC Motor Control eTPU Function Set (set3),” AN2958
14. eTPU Graphical Configuration Tool, http://www.freescale.com , search keyword “ETPUGCT”
15. “DSP56F80x MC PWM Module in Motor Control Applications,” AN1927

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004. All rights reserved.