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Application Note

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Differences Between Controller Continuum ADC Modules

12-bit ADC vs. 16-bit ADC

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1 Introduction

The 16-bit SAR ADC module is the latest embedded ADC to be integrated into the Controller Continuum families. The differences between this 16-bit SAR ADC and the previous 12-bit SAR ADC are more than just an extension to the result register. This document explains what the differences are and how to use the new 16-bit ADC module in the traditional method.

If you wish to make use of the 16-bit ADC's extended functions, incorporating calibration and the programmable delay block hardware triggers, refer to the Freescale application note titled *ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* (document AN3949) which addresses these new features or the Freescale quick reference guide titled *Quick Reference User Guide for Analog Peripherals for the MM Family.* The application note AN3949 also includes driver files and code examples for the MCF51EM256 16-bit ADC to

Contents

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initialize and use the ADC and PDB. This includes calibration and synchronization functions.

NOTE

With the exception of mask set errata documents, if any other Freescale document contains information that conflicts with the information in the device reference manual, the reference manual should be considered to have the most current and correct data.

2 Feature Comparison

The 12-bit ADC (as seen on devices such as the MCF51QE128) and the 16-bit ADC (as seen on the MCF51EM256, MCF51MM256, and MC9S08MM128) are both successive approximation analog-to-digital converters. See Figure 1. They consistof sample-and-hold circuitry to acquire the input voltage (V_{In}), a comparator, a successive approximation register sub-circuit, and an internal reference capacitive DAC. This DAC supplies the comparator with an analog voltage equivalent of the digital code output of the SAR, for comparison with V_{In}.

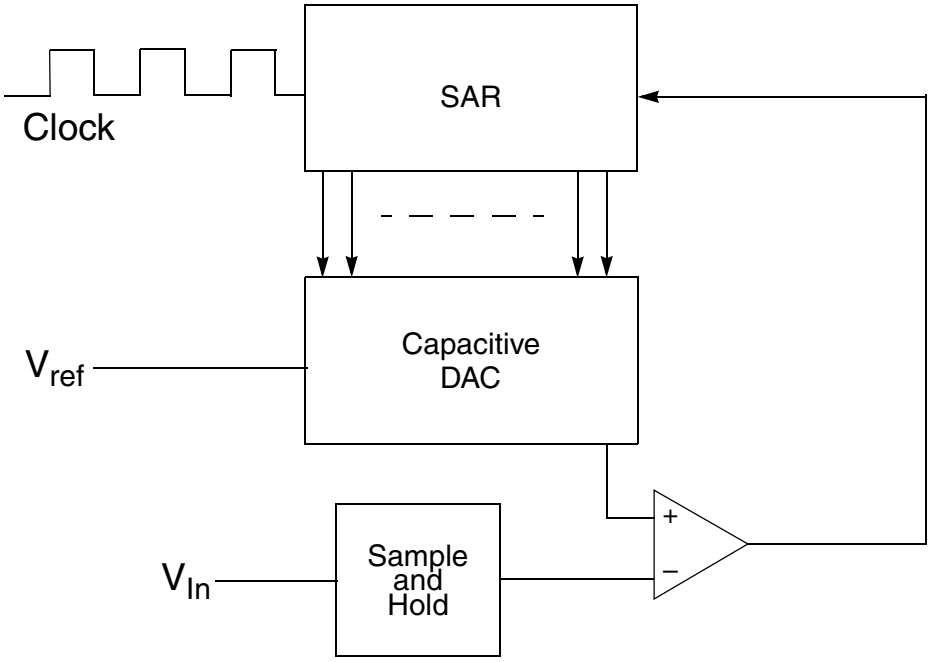

Figure 1. SAR ADC block diagram (functional)

A summary of the key features of both the outlined ADCs are summarized in Table 1.

Table 1. Summary of key features

Feature	12-bit ADC	16-bit ADC
Method	Linear SAR	Linear SAR
Resolution	12, 10, and 8	16, 12, 10, and 8
Single-ended inputs	Yes[1]	Yes[1]
Differential inputs	No	Yes[1]

Table 1. Summary of key features (continued)

Single and continuous conversions	Yes	Yes
Configurable sample time and conversion speed	Yes	Yes
Input clock sources	Up to 4	Up to 4
Operation in power-saving modes	Yes	Yes
Hardware trigger	Yes, device dependent	Yes, device dependent
Compare function	Yes	Yes
Temperature sensor	Yes	Yes
Hardware averaging	No	Yes
Voltage reference	Fixed	Selectable
Self-calibration	No	Yes
Supply voltage	1.8–3.6 V	1.8–3.6 V
Maximum conversion clock frequency	8.0 MHz	TBD

[1] The number is dependant on the device.

Key points to note are that the 16-bit ADC supports differential input as well as the standard single-ended channels, whereas the 12-bit ADC supports only single-ended channels. The 16-bit ADC can be configured to provide right-justified 12-bit, 10-bit, or 8-bit results for backwards compatibility with the 12-bit ADC. However, the 16-bit ADC has additional features, such as averaging, selectable voltage references, and calibration features, that can be configured to maintain backwards compatibility with the 12-bit ADC.

3 Operational Differences

3.1 Enabling the Module

In general terms there are no differences in enabling the ADC modules. They both have the same clock gating schemes implemented. The ADCs are enabled or disabled by the ADCH bits in the status and control register 1 (ADCSC1n). If all the bits in ADCSC1n are set then the module is disabled. The Freescale quick reference user guide titled *QE128 Peripheral Module Quick Reference User Guide*, (document QE128QRUG) give some examples of initialization and usage.

The main difference in module enablement is the 16-bit ADC calibration function. This calibration is required to achieve the accuracy specified in the datasheet, but it is not a requirement for general operation. See Section 4.1, “ADC Accuracy,” for more details on accuracy specifications. The calibration process is explained further in Freescale application note titled *ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* (document AN3949) or the *Quick Reference User Guide for Analog Peripherals for the MM Family.*

NOTE

An uncalibrated 16-bit SAR ADC will not meet the device’s accuracy specification given in the data sheet.

3.1.1 ADC Input Pin Enablement

ADC input pins are generally multiplexed with general purpose I/O and other functions to increase device flexibility. As a result ADC inputs share pads with other functions. Due to differences in analog and digital function, if a pin is to be used as an ADC input this analog function must be enabled.

The 12-bit ADC controls this enablement via the analog pin control registers (APCTL1:N). Both the pin control register and the ADC channel must be enabled and selected for an ADC conversion to complete successfully.

Conversely, pin muxing on the 16-bit ADC is controlled by the Port Pin Function bit field in the PTxPFn registers in the GPIO register block. Both the Port Pin Function Register and the ADC channel must be selected for an ADC conversion to complete successfully.

A code example showing how to enable the 16-bit ADC pins is provided in the software accompanying the application note *ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* (document AN3949) or the *Quick Reference User Guide for Analog Peripherals for the MM Family.*

3.2 Initializing the Module

There are significant differences in the registers and their initialization. The code written for the 12-bit ADC may compile successfully with only a few small modifications to names for header file compatibility. However, although most bit settings are designed to default to a backward compatible mode, care must be taken to check each bit field to ensure that the ADC operates properly.

3.2.1 Registers

The most obvious difference between the 12-bit and 16-bit ADC modules is the inclusion of a second status and control register (ADCSC1B) and ADCSC3 in the 16-bit module. Table 2 summarizes all the status, control, and configuration bit field locations, with respect to the register name and their default configurations.

Table 2. Bit field location and default setting

Bit field name	Description	12-bit location	16-bit location	Default
COCO	Conversion complete	ADCSC1	ADCSC1n[1]	n/a
AIEN	Interrupt enable	ADCSC1	ADCSC1n[2]	Disabled
DIFF	Differential mode	n/a	ADCSC1n[2]	Single ended
ADCH	Channel	ADCSC1	ADCSC1n[2]	Module disabled
ADLPC	Low power conversion	ADCCFG	ADCCFG1	Normal/Off
ADIV	Clock divider	ADCCFG	ADCCFG1	TBD
ADLSMP	Long sample	ADCCFG	ADCCFG1	Short
MODE	Conversion mode	ADCCFG	ADCCFG1	8-bit
ADICLK	ADC clock select	ADCCFG	ADCCFG1	Bus clock
ADACKEN	Alternate clock enable	n/a	ADCCFG2	Disabled

Table 2. Bit field location and default setting (continued)

ADHSC	High speed conversion	n/a	ADCCFG2	Normal/Off
ADLSTS	Long sample time select	n/a	ADCCFG2	Longest
ADACT	Conversion active	ADCSC2	ADCSC2	n/a
ADTRG	Trigger mode	ADCSC2	ADCSC2	Software
ACFE	Compare function enable	ADCSC2	ADCSC2	Disabled
ACFGT	Compare function greater than	ADCSC2	ADCSC2	Less than
ACREN	Range enable	n/a	ADCSC2	Disabled
REFSEL	Voltage reference select	n/a	ADCSC2	V_{REFH} and V_{REFL}
CAL	Calibration	n/a	ADCSC3	Off
CALF	Calibration fail flag	n/a	ADCSC3	n/a
ADCO	Continuous conversion	ADCSC1	ADCSC3	Single conversion
AVGE	Averaging enable	n/a	ADCSC3	Disabled
AVGS	Averaging select	n/a	ADCSC3	4 samples

1 "n" refers to either register A or B

3.2.1.1 Status Control and Configuration Register Differences

The 16-bit ADC hasup to eight sets of ADCSC1 registers. Each bit field in the register also has the same letter notation at the end for increased visibility. In other words, the COCO bit is called COCOA in ADCSC1A and COCOB in ADCSC1B. There are two sets of registers due to the MCF51EM256 ADC's implementation and integration with the PDB module as the hardware trigger, which therefore initiates two conversions (A and B) from a single periodic hardware trigger. This means that two status and control registers are required to configure the conversion channels and provide independent results.

Information on how to use these triggers is provided in the application note *ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* (document AN3949) or the *Quick Reference User Guide for Analog Peripherals for the MM Family.*

There are eight sets of registers due to the MCF51MM256 and MC9S089MM128 ADC's implementation and integration with the PDB module as the hardware trigger that can initiate eight conversions (A through H) from a single periodic hardware trigger. This means that eight status and control registers are required to configure the conversion channels and provide independent results.

The ADCO bit, which controls whether the ADC performs single or continuous conversions, has moved from ADCSC1 on the 12-bit ADC implementation to ADCSC3 on the 16-bit ADC implementation.

The 16-bit ADC has enhanced functionality through the inclusion of more options such as enhanced conversion time configuration and the inclusion of a range function. This range function has to be used in conjunction with the compare option to allow two limits — high and low — of a result, instead of just one as on the 12-bit ADC.

3.2.1.2 Result Register Differences

The 16-bit ADC has up to eight result registers for the same reason as the second ADCSC1 register. The 16-bit result registers (ADCRH:L) operate in single-ended mode the same way as the 12-bit ADC, with unsigned right-justified data. The 16-bit ADC in differential mode records the data in the result register in sign-extended two's-complement format.

3.2.1.3 Compare Value Registers

The use of the compare value registers is identical between the 12-bit ADC and 16-bit ADC if the 16-bit range function is disabled (ACREN = 0) and the single-ended mode is in use for backward compatibility. When using this feature in differential mode (ACREN=0), the value set in the compare register must be in the same format as the result register, in other words sign-extended right-justified two's-complement. The second 16-bit compare value register is only used if the range function is enabled. Table 3 summarizes all the configurations of the compare function on the 16-bit ADC and 12-bit ADC. Here X denotes "does not care."

Table 3. Compare function configurations

ACFE	ACFGT	ACREN	ADCCV1	ADCCV2	Function	12-bit ADC Supported
0	X	X	X	X	Disabled	Yes
1	0	0	Target Result	X	Less Than	Yes
1	1	0	Target Result	X	Greater or Equal	Yes
1	0	1	$\leq$ CV2	> CV1	Outside Range	No
1	0	1	> CV2	$\leq$ CV1	Inside Range	No
1	1	1	$\leq$ CV2	> CV1	Inside Range Inclusive	No
1	1	1	> CV2	$\leq$ CV1	Outside Range Inclusive	No

3.2.1.4 Offset, Gain and General Calibration Registers

The 12-bit ADC has no support for offset or gain manipulation through calibration or otherwise. If you wish to make use of the 16- bit ADCs calibration, offset, and gain functions, refer to the Freescale application note *ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* (document AN3949) which address these new features or the *Quick Reference User Guide for Analog Peripherals for the MM Family.*

3.3 Initiating Conversions

After the module is configured with the selected setting, both modules can initiate conversions via software or hardware trigger.

3.3.1 Software Triggers

If configured for a software trigger, writing the channel number to the appropriate ADCH register initiates a conversion. If continuous conversions are enabled, further conversions start when the previous result is transferred into the result register from the SAR shown in Figure 1.

3.3.2 Hardware Triggers

The hardware trigger source is variable depending upon device integration. Typical hardware trigger sources are timers and comparators. Details of the hardware trigger source are found in the ADC module introduction in the appropriate reference manual.

3.4 Completing Conversions

Completed conversions are indicated by the COCO flag. This is set after every conversion unless averaging or the compare function is enabled. To avoid any loss of data, the result must be read before another conversion is started in single-conversion mode, or before another conversion completes in continuous-conversion mode. This loss of data is a result of the blocking mechanism which is in place (in any mode >8-bits) to prevent the ADC overwriting and corrupting a result that is in the process of being read. This blocking mechanism is needed due to the fact that the result register is in fact two 8-bit registers read independently.

If the compare function is enabled, the COCO flag only sets when the event occurs, not after each conversion. In single-conversion mode, this means that the software must initiate further conversions until the compare event has occurred. This function is the same for both ADCs.

When the 16-bit ADC is set up for compare and averaging, the COCO bit is set only when both conditions are met.

If interrupts are enabled, the setting of the COCO flag will also generate the corresponding interrupt.

3.5 New Features

The features described here are new on the 16-bit ADC and not supported on previous ADC versions. The default condition of the function is highlighted in Table 2.

3.5.1 Calibration, Including User-Defined Offset and Gain

The 16-bit ADC requires self-calibration to be run after every reset to ensure that the specified accuracies in the data sheet are met. This one-time calibration must be done to generate the offset and gain calibration values. These values are automatically subtracted and multiplied during the conversion sequence to compensate for errors as shown in Figure 2. The offset registers are also user-configurable for custom offset.

Further details about the calibration feature can be found in Freescale application note *ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* (document AN3949) or the *Quick Reference User Guide for Analog Peripherals for the MM Family.*

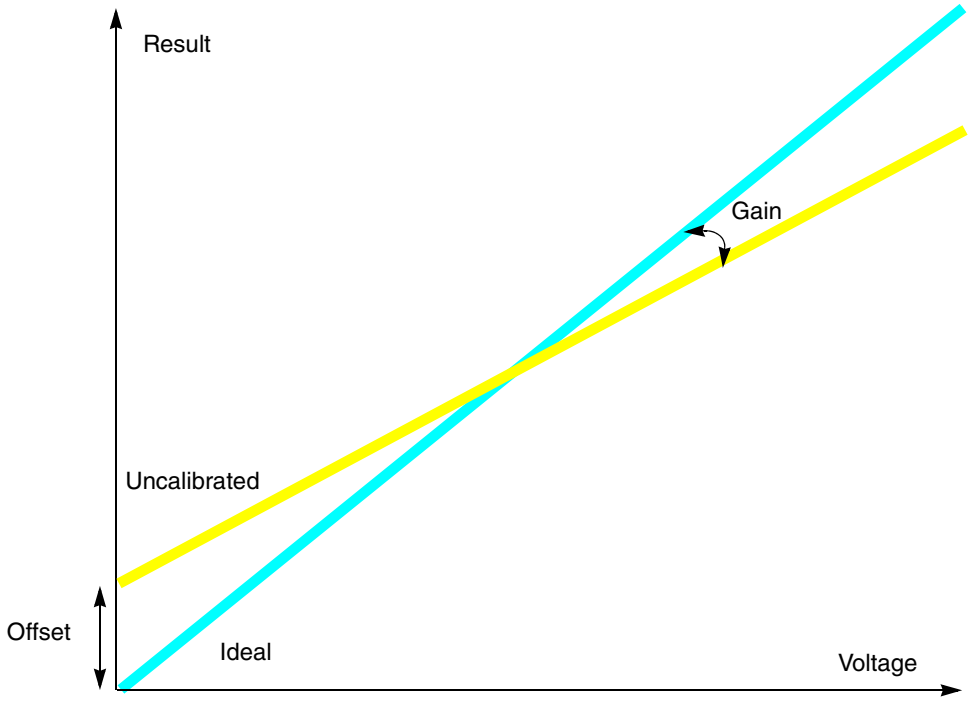

Figure 2. Gain and offset effect on result

3.5.2 Conversion Speed

The 16-bit ADC has more configurable speed options than its predecessors. ADACKEN, ADHSC, ADLSTS, and AVGE are new features that affect the conversion time (time between conversion initiation and the COCO flag being set).

- Asynchronous clock output enable (ADACKEN)—Allows the user to enable or disable the asynchronous clock output. This has no effect while the ADC is running off of a bus-driven source. If the asynchronous clock is being used as the ADC clock source (a requirement for operation in Stop3 mode), this switch allows you to have the ADACK running regardless of the state of the ADC, or running only while a conversion is active. This second option induces a delay to the conversion completion via the Single or First Continuous Time Adder (SFCAdder) due to the clock switching delay as described in the sample time and total conversion time section of the reference manual.
- High speed configuration (ADHSC)—This bit is a setting which adds four ADCK cycles to the conversion sequence to allow high-speed operation.
- Long sample time select (ADLSTS)—Is a bit field that prolongs the sample time of the SAR when the long sample time (ADLSMP = 1) is selectable as 0 (off), 2, 6, 12, or 20 ADCK extra cycles. The 12-bit ADC long sample time adder (LSTAdder) is only configurable as on (20 cycles) or off (0 cycles). The default condition is shown in Table 2.
- AVGE—The averaging function (enabled via AVGE) also has an effect on the conversion time as it multiplies the base conversion time plus any speed adders. Equation 1 shows the 12-bit ADC's conversion time formula, whereas Equation 2 shows the 16-bit ADC's formula, with differences highlighted in italics.

12-bit:

$$ConversionTime = SFCAdder + BCT + LSTAdder \quad \textit{Eqn. 1}$$

16-bit:

$$ConversionTime = SFCAdder + AverageNum(BCT + LSTAdder + HSCAdder) \quad \textit{Eqn. 2}$$

In this case SFCAdder is the single or first conversion adder and BCT is the base conversion time. A summary of the effects these choices have on the conversion time are detailed in Section 4.2, "ADC Conversion Timings."

3.5.3 Averaging

The 16-bit ADC has the added feature of averaging. Averaging can be used to reduce conversion error due to the system noise. In this case the COCO bit is set after the set of conversions (4, 8, 16, or 32) have completed. In single conversion mode the conversion initiation starts the first conversion and keeps initiating conversions (in the hardware, not by the software) until the set is complete.

3.5.4 Differential Input

The differential inputs can be configured as right-justified two's-complement values: 16-bit, 13-bit, 11-bit, or 9-bit. The ADC result register will hold the magnitude of difference between the plus side (DADP0:3) and minus side (DADM0:3) input pins. If DADPn is greater than DADMn the result is positive, and in the opposite case the result is negative.

3.5.5 Voltage Reference

Unlike the 12-bit ADC which does not have a selectable voltage reference, the 16-bit SAR ADC has the option to select the ADC supply voltage reference via the REFSEL bit field. The default is the backward compatible setting of the external pins V_{REFH} and V_{REFL}.

The voltage reference can be changed to reference against the internal bandgap voltage (the bandgap buffer must be enabled in the System Power Management Status and Control 1 register SPMSC1) $V_{BGH:L}$ pair from the voltage regulator or to the alternative reference, $V_{ALTH:L}$ pair, which is the trimmable Vref module output.

4 Accuracy and Timing Specifications

Both versions of the ADC modules discussed in this document have different accuracy specifications and conversion timings. This does not have a large impact on functionality but does bear an effect on the performance of the system.

4.1 ADC Accuracy

Both the 12-bit and 16-bit ADC modules on the QE128 devices have similar features, specifications, and operation. Looking at the electrical characteristics in the datasheets quickly illustrate the improved resolution that the 16-bit ADC has, even in the 12-bit operation mode. The graph below shows key figures (for the ADC's single ended mode) in the LSB and then in milivolts based on a 3 V supply.

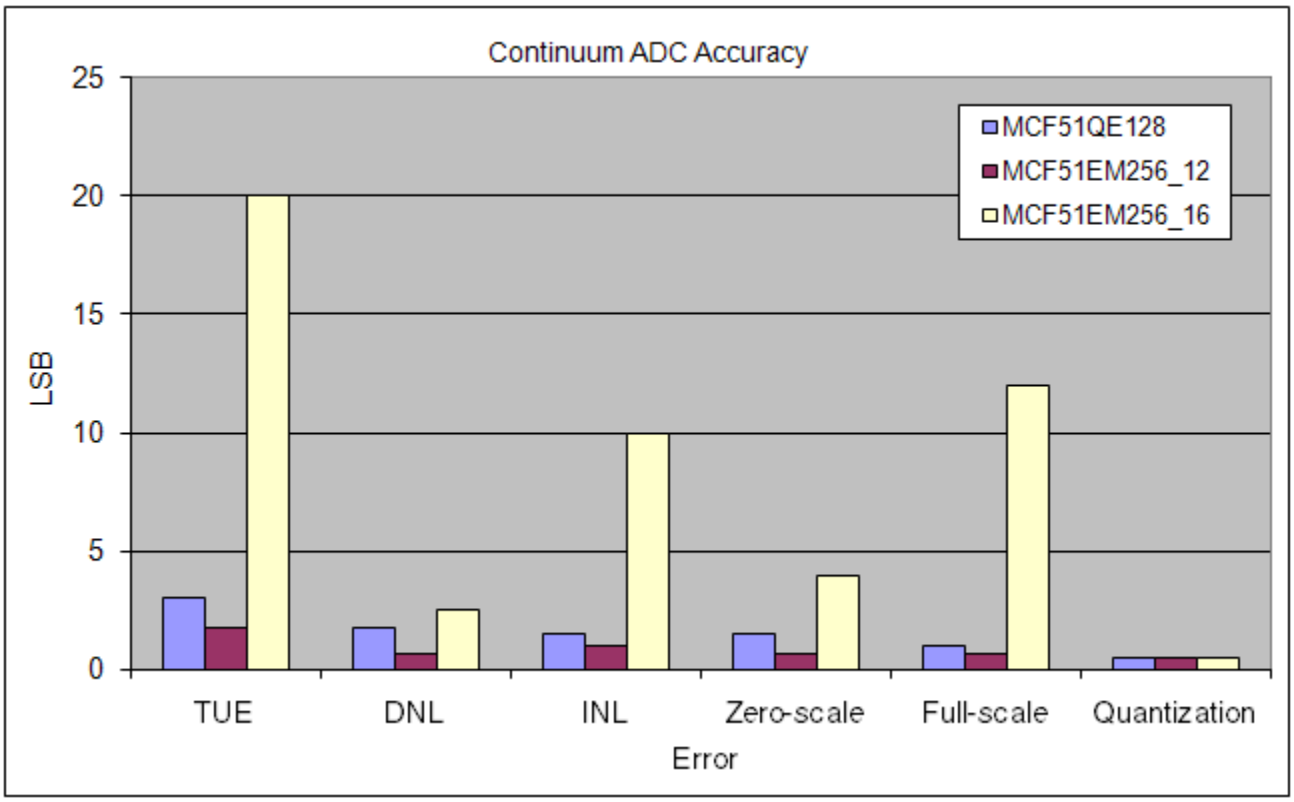

Figure 3. ADC errors expressed as LSB

The graphs in Figure 3 and Figure 4 show that care must be taken to translate the LSB figures to real values to compare fairly. In the case of the 16-bit ADC the 12-bit mode has a better TUE LSB figure, but when you look at the real meaning of that number in the mV, the opposite conclusion is made. The choice must be made on the system requirements of the application, resolution, and accurracy in the absolute voltage or LSB.

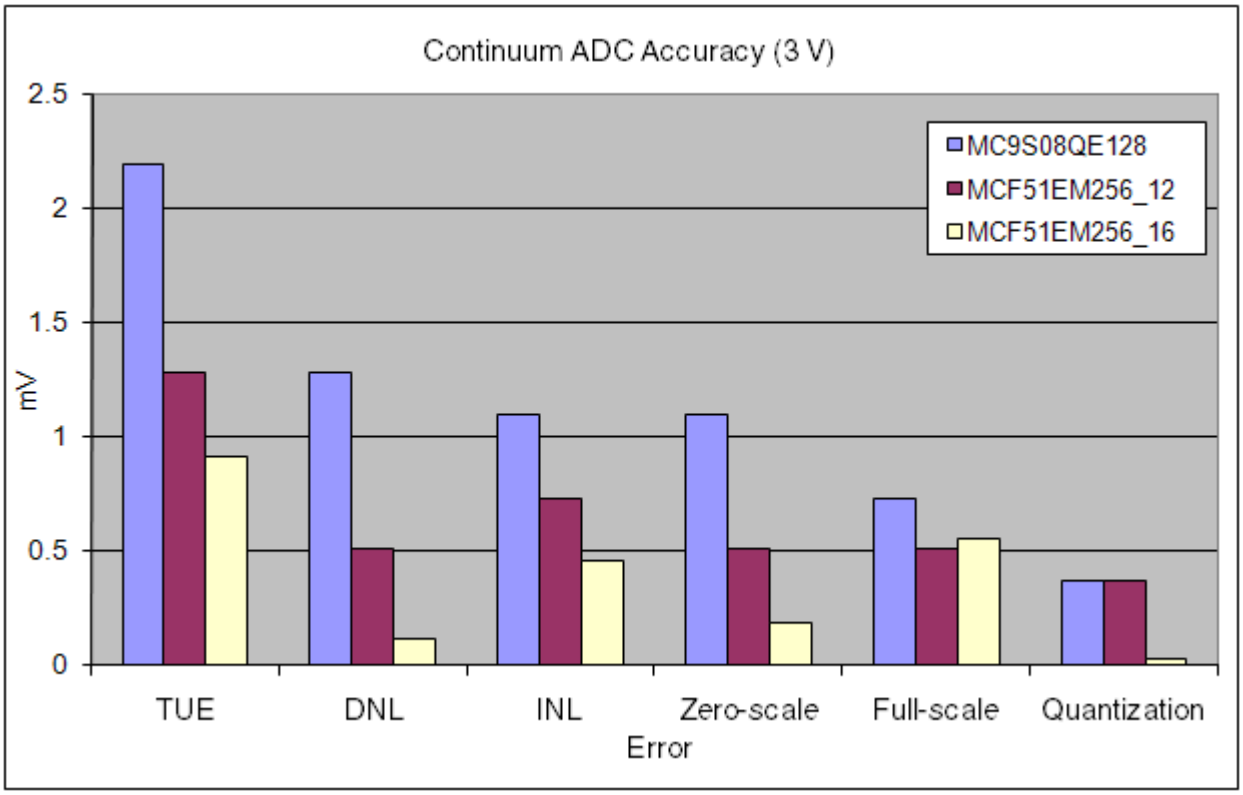

Figure 4. ADC errors expressed as mV on a 3 V supply voltage

4.2 ADC Conversion Timings

Section 3.5.2, "Conversion Speed," describes how the conversion time is calculated. The next three tables compare the 16-bit and 12-bit ADC's conversion time factors for all available user settings.

Table 4 shows that the base conversion times for both ADC modules are the same in common modes.

Table 4. Base conversion time

Mode	Base conversion time (ADC16)	Base conversion time (ADC12)
8-bit SE	17 ADCK cycles	17 ADCK cycles
9-bit DIFF	27 ADCK cycles	N/A
10-bit SE	20 ADCK cycles	20 ADCK cycles
11-bit DIFF	30 ADCK cycles	N/A
12-bit SE	20 ADCK cycles	20 ADCK cycles
13-bit DIFF	30 ADCK cycles	N/A
16-bit SE	25 ADCK cycles	N/A
16-bit DIFF	34 ADCK cycles	N/A

Table 5 highlights that the single or first continuous time adder (SFCAdder) does differ between module versions. Selecting ADACK adds 5 µs to the conversion time of the 12-bit ADC, whereas on the 16-bit

ADC the addition of 5 µs occurs only if it is enabled for the conversion, then disabled to save power between conversions. The 16-bit ADC SFCAdder depends on the setting of ADLSMP. This is not the case for the 12-bit ADC.

Table 5. Single or first conversion time adder

ADACKEN	ADLSMP	ADICLK	Single or first continuous adder (ADC16)	Single or first continuous adder (ADC12)
X	1	Other	3 ADCK cycles + 5 bus cycles	3 ADCK cycles + 5 bus cycles
1	1	ADACK	3 ADCK cycles + 5 bus cycles	3 ADCK cycles + 5 bus cycles + 5 µs
0	1	ADACK	3 ADCK cycles + 5 bus cycles +5 µs	N/A
X	0	Other	5 ADCK cycles + 5 bus cycles	3 ADCK cycles + 5 bus cycles
1	0	ADACK	5 ADCK cycles + 5 bus cycles	3 ADCK cycles + 5 bus cycles + 5 µs
0	0	ADACK	5 ADCK cycles + 5 bus cycles + 5 µs	N/A

As mentioned previously the long sample time adder is programmable on the 16-bit ADC, where it is fixed at 20 ADCK cycles for the 12-bit ADC.

Table 6. Long sample time adder

ADLSMP	Conversion time adder (ADC16)	Conversion time adder (ADC12)
0	0 ADCK cycles	0 ADCK cycles
1	Selectable 2, 6, 12, 20 ADCK cycles	20 ADCK cycles

The 16-bit ADC also has a selectable high speed adder of 4 ADCK cycles and an averaging option of 1, 4, 8, 16, or 32 times.

The application of these settings to the conversion times is shown in Equation 1 and Equation 2.

5 Conclusion

Freescale's new 16-bit ADC for embedded microcontrollers is an evolutionary step from the previous 12-bit ADC used on the Flexis families. Although the 16-bit ADC has many enhancements from the 12-bit ADC, this is a natural progression and must not be an obstacle for programmers and designers familiar with the 12-bit ADC's functionality and features.

6 References

- Application note—*ADC 16 Calibration Procedure and Programmable Delay Block Synchronization for the MCF51EM256* document AN3949.
- Reference Manual—*MCF51EM Family ColdFire® Integrated Microcontroller Reference Manual*, document MCF51EM256RM.
- Data sheet—*MCF51EM256/128MCF51EM32 ColdFire Microcontroller Data Sheet*, document MCF51EM256, Rev. 0, date March 2009, *Quick Reference User Guide for Analog Peripherals for the MM Family.*
- Reference Manuals—*MM256 and MM128*

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