NXP Semiconductors
Application Note

Document Number: AN4829
Rev. 0, 07/2017

Common Board Design between T1024 and T1022 Processor

Contents

1 About this document

This document explains how to design a common board between T1024 and T1022 QorIQ communications processor by achieving hardware compatibility.

Common board here implies that T1024 or T1022 can be populated without any board layout rework requirement. Alternative designs of the common board are possible; it is recommended to contact NXP representatives for details of validation.

NOTE

T1022 recommendations in this document also applies to T1042 however differences are mentioned wherever applicable.

2 Chip feature comparison

The figure below shows the block diagram for T1024.

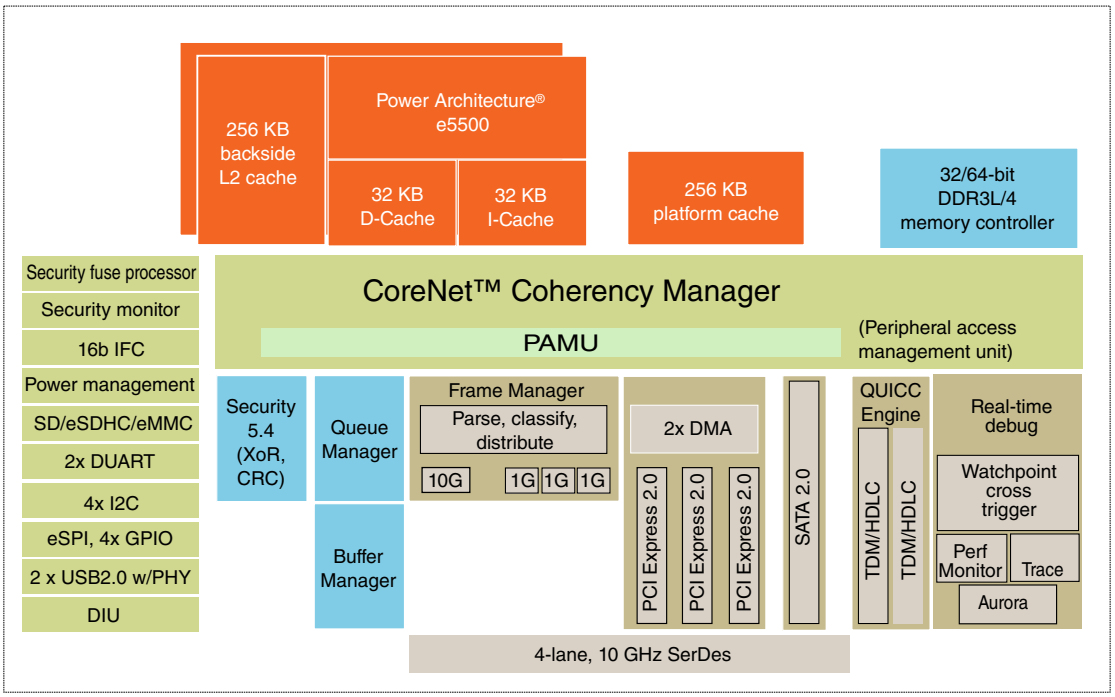

Figure 1. T1024 block diagram

The figure below shows the block diagram for T1022.

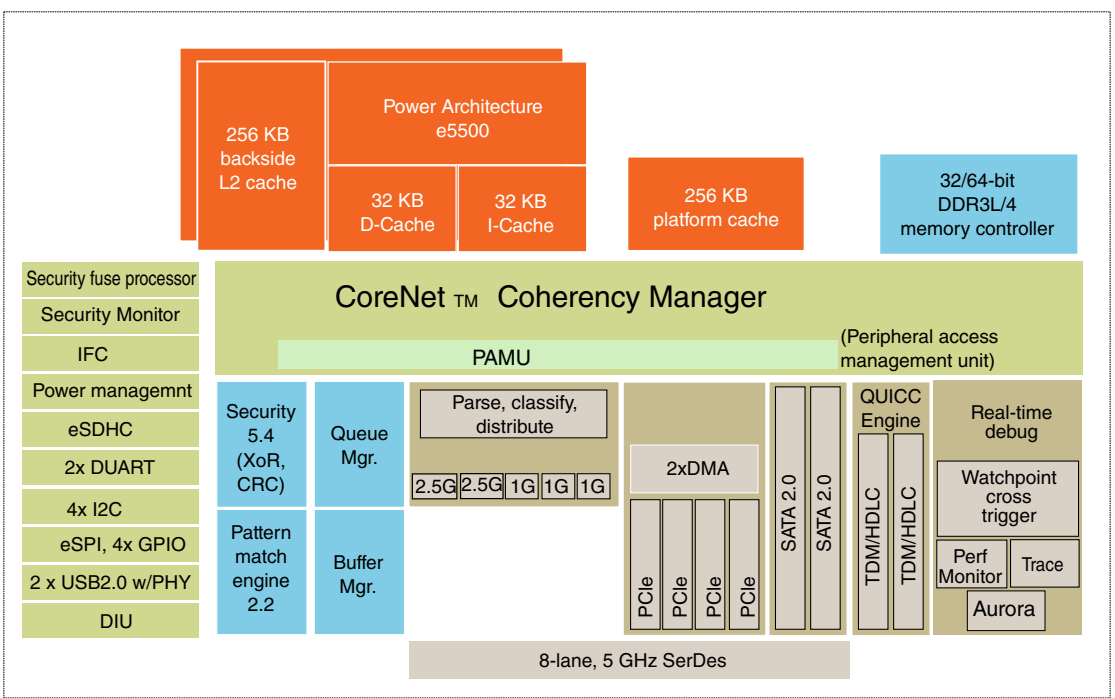

Figure 2. T1022 block diagram

The figure below shows the block diagram for T1042.

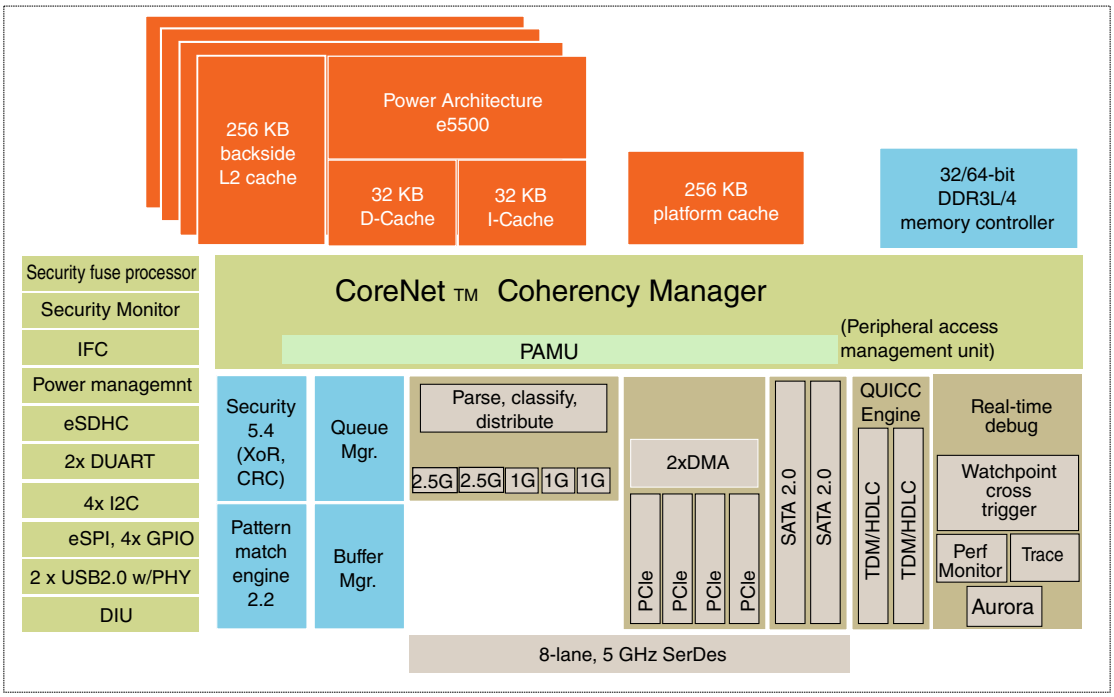

Figure 3. T1042 block diagram

This table compares T1024 and T1022. Differences between chips are shaded.

Table 1. Detailed chip feature comparison

Features	T1024	T1022	T1042
Cores			
Number of cores	2 x e5500 Power Architecture	2 x e5500 Power Architecture	4 x e5500 Power Architecture
Architecture width	64-bit	64-bit	
Max frequency (MHz)	1400	1400	
DMIPS/MHz	3	3	
Memory Size			
L1 cache	32 KB I/D	32 KB I/D	
L2 cache	256 KB per core backside	256 KB per core backside	
CoreNet platform cache (CPC)	256 KB frontside	256 KB frontside	
Cache-line size	64 bytes	64 bytes	
Main memory type	1 x DDR3L/4 1600 MT/s	1 x DDR3L/4 1600 MT/s	
Maximum size of main memory	32 GB (1 Gbit x 8 device)	32 GB (1 Gbit x 8 device)	
I/O			
Ethernet controllers	1x 10 Gbps XFI; 1x QSGMII; 3x 1 Gbps SGMII; 2x RGMII	5x 1 Gbps SGMII; 2x 2.5 Gbps SGMII; 2x RGMII; 1x MII	
SerDes lanes	4 lanes at up to 10 GHz	8 lanes at up to 5 GHz	
PCI Express controllers	3 x Gen 2.0 controllers; 5 Gbps	4 x Gen 2.0 controllers; 5 Gbps	
SATA	1 x SATA controllers up to 3.0 Gbps operation	2 x SATA controllers up to 3.0 Gbps	

Table continues on the next page...

Table 1. Detailed chip feature comparison (continued)

Features	T1024	T1022	T1042
TDM	Supported through QE-TDM only	Supported	
Display Interface Unit	12 bit dual data rate	12 bit dual data rate	
QE	HDLC, Transparent UART, TDM/SI	HDLC, Transparent UART, TDM/SI	
Integrated Flash Controller (IFC)	8-/16-bit data width, 32-bit address width	8-/16-bit data width, 32-bit address width	
Clocking			
Single source clocking	DIFF_SYSCLK/ DIFF_SYSCLK_B supported	DIFF_SYSCLK/ DIFF_SYSCLK_B supported	
Power Management			
Deep Sleep	Supported	Supported	
Package			
Package	23mm X 23mm, 0.8mm pitch, 780 pin FC-PBGA	23mm X 23mm, 0.8mm pitch, 780 pin FC-PBGA	

3 Pin-compatibility options

This section elaborates on the hardware, and board-level differences that exists when migrating between T1024 and T1022, particularly items that are critical to the hardware design engineer. If proper attention is taken and a common feature set is utilized between the chips, it is possible to design a platform that supports both the chips.

This figure highlights the differences between T1024 and T1022 chip packages.

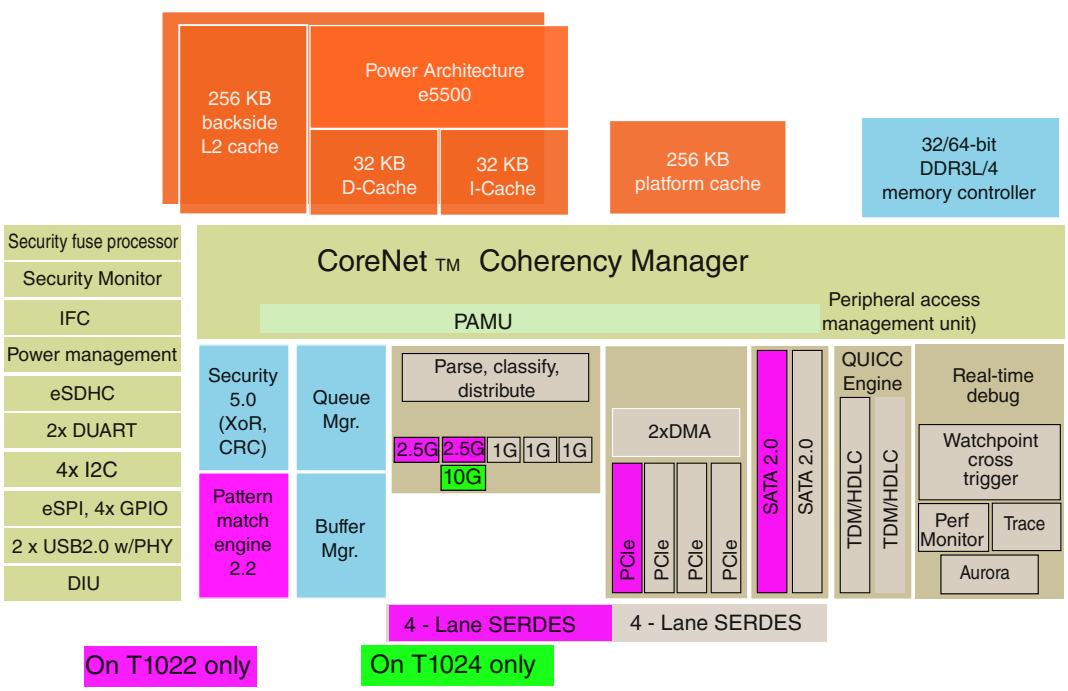

Figure 4. Device compatibility between T1024 and T1022 chip packages

NOTE

In the above figure, Green highlighting indicates features that are unique to T1024 chip package, and magenta highlighting indicates features that are unique to T1022 chip package.

3.1 Achieving full pin-compatibility

In some interfaces, full pin-compatibility is possible between T1024 and T1022. This table lists the interfaces for which full pin compatibility is possible, with a cross-reference to the related section that describes the procedure for full pin compatibility.

Table 2. Full-pin-compatible interfaces

Interface	Compatibility procedure section
DDR, DIU, eSPI, DUART, QE	Identical interfaces

This table lists the interfaces that can be made compatible for migration, but for which full pin compatibility is not possible. It also has a cross-reference to the related section that describes the procedure for migration compatibility.

Table 3. Partial-pin-compatible interfaces

Interface	Compatibility procedure section
IFC	IFC recommendations
USB	USB controller recommendation
Ethernet controller	Ethernet controller recommendation
DMA	DMA recommendation
I2C	I2C recommendation
eSDHC	eSDHC recommendation
SerDes	SerDes recommendations
Ethernet MACs	Ethernet MACs options
Power Management	Power management recommendations
Power Islands	Power island requirements
DFT	TEST_SEL_B requirements
MPIC	MPIC requirements

4 Interface-specific compatibility

This section describes the specific connections and software settings required for full and partial pin-compatibility between the various controllers and power supply interfaces on T1024 and T1022 chip families.

4.1 Identical interfaces

The following interfaces are identical between T1024 and T1022:

- Display Interface Unit (DIU)
- Enhanced SPI controller (eSPI)
- DUART controller
- JTAG

4.2 DDR controller recommendations

T1024 supports 16-/32-/64-bit DDR3L and 32-/64-bit DDR4 controller.

T1022 supports 32-/64-bit DDR3L and 64-bit DDR4 controller. Refer to the device datasheet and Chip errata document for more details.

4.3 IFC recommendations

T1024 supports IFC_CS_B[0:6] and T1022 supports IFC_CS_B[0:7]. T1022 supports 32-bit address along with 8 chip select whereas T1024 supports following options:

Table 4. IFC pin muxing options on T1024

Options	Address	Chip Select
1	32-bits	IFC_CS_B[0:3]
2	25-bits	IFC_CS_B[0:6]

NOTE

Refer Table 13 for pin selection.

4.4 USB controller recommendation

USBCLK is muxed with IRQ1 in T1024 selectable through RCW bits. In T1022, USBCLK is available on dedicated pin.

USB controller provides the option to select clock from USBCLK or reference clock generated internally from system clock. This can be achieved through programming USB PHY registers.

For common board design, use of "Single Oscillator Source" reference clock mode is recommended.

4.5 Ethernet controller recommendation

EC1 interface in RGMII mode is fully pin compatible between T1024 and T1022 however t_{SKRGT_RX} parameter in AC timing specifications of the devices does not cover the same timing window. Refer to T1024 and T1022 datasheet for more details.

To meet t_{SKRGT_RX} timings on common board design, use a combination of data to clock delay using PHY pad delay and alternate trace delay paths on PCB for T1024 and T1022 device timing requirements.

The alternate trace delays on PCB can be implemented as shown in following figure.

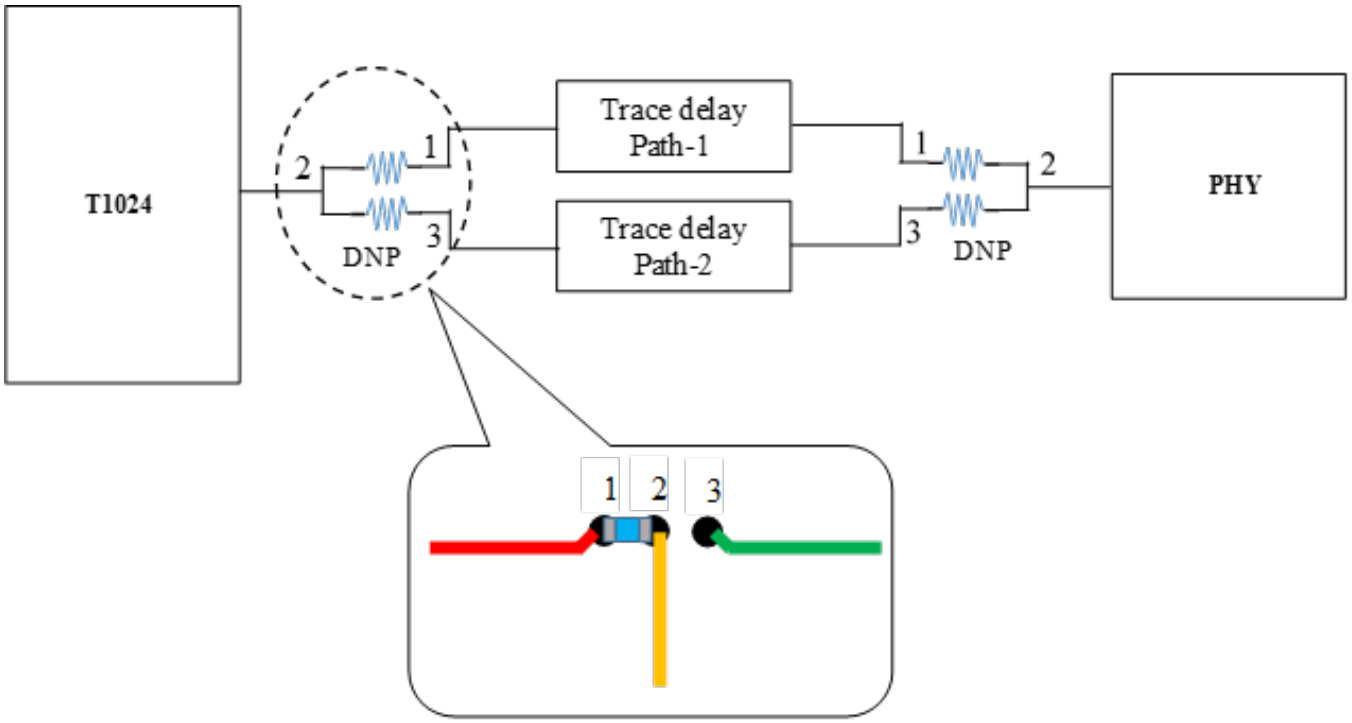

Figure 5. Selecting alternate trace path using 3-pin pad

For common board design, EC1 MII mode (T1022 only) should not be used.

EC2 is not pin compatible between T1024 and T1022 and it is not recommended to be used on common board design.

4.6 DMA recommendation

External DMA pins are not pin compatible between T1024 and T1022 and it is not recommended to be used on common board design.

4.7 I2C recommendation

I2C1, I2C2 and I2C4 are pin compatible between T1024 and T1022, however I2C3 is mapped as shown in Table 13. I2C3 is not recommended to be used between T1024 and T1022 on common board design.

I2C2 is muxed with GPIO in T1024 which is not available in T1022. Use I2C2 option only on common board design.

4.8 eSDHC recommendation

SDHC_VS pin is not pin compatible between T1024 and T1022, see Table 13. For common board design, it is recommended to use legacy modes (default and high speed SDHC modes) which do not use these signals or implement external multiplexer to select SDHC_VS signal between T1024 and T1022 as shown in the this table.

Table 5. SDHC_VS pin selection

Package pin	T1024	T1022
D3	SDHC_VS	IRQ01
D1	NC	SDHC_VS

This figure below explains the method to multiplex signals between SDHC_VS of T1024 and SDHC_VS of T1022.

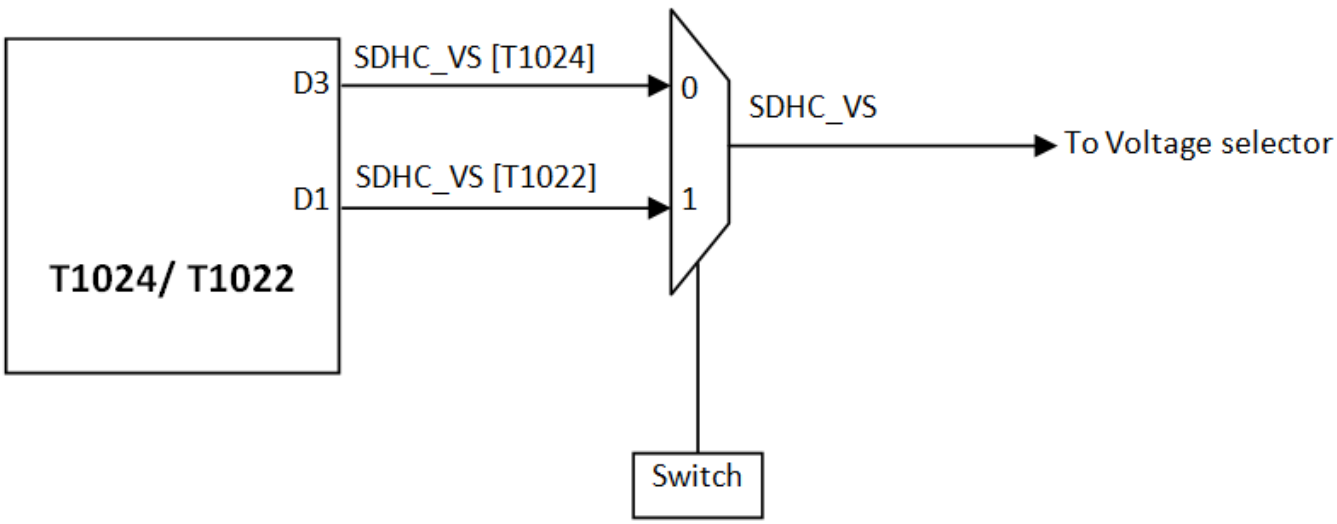

Figure 6. SDHC_VS pin multiplexer

4.9 QE interface recommendation

QE interface is pin compatible between T1024 and T1022

4.10 SerDes recommendations

The XFI protocol is not compatible on T1024 and T1022.

4.10.1 Compatible SerDes-muxing options

T1022 has 8 SerDes lanes whereas T1024 has only 4 lanes. The upper lanes (E, F, G, H) of T1022 are mapped to T1024 lanes.

This table shows SerDes assignments applicable to T1022 only . For nomenclature, refer QorIQ T1040 Reference Manual.

Table 6. SerDes assignments applicable to T1022 only

SRDS_PRCTL_S1 RCW[128:135]	A	B	C	D	E	F	G	H
0x86	PCIe1	sg.m3	sg.m1	sg.m2	PCIe2	PCIe3	PCIe4	SATA.1

Table continues on the next page...

Table 6. SerDes assignments applicable to T1022 only (continued)

SRDS_PRCTL_S1 RCW[128:135]	A	B	C	D	E	F	G	H
	(5/2.5)				(5/2.5)	(5/2.5)	(5/2.5)	(3/1.5)
0x87	PCIe1 (5/2.5)	sg.m3	sg.m1	sg.m2	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	sg.m5
0x45	PCIe1 (5/2.5)		sg.m1	sg.m2	PCIe2 (5/2.5)		sg.m4	sg.m5
0xA7	PCIe1 (5/2.5)	sg.m3	sg.m1 (2.5G)	sg.m2 (2.5G)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	sg.m5
0x06	PCIe1 (5/2.5)				PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA.1 (3/1.5)
0x08	PCIe1 (5/2.5)				PCIe2 (5/2.5)	PCIe3 (5/2.5)	SATA.2 (3/1.5)	SATA.1 (3/1.5)
0x8E	PCIe1 (5/2.5)	sg.m3	sg.m1 (2.5G)	sg.m2	Aurora	PCIe3 (5/2.5)	sg.m4	SATA.1 (3/1.5)
0x85	PCIe1 (5/2.5)	sg.m3	sg.m1 (2.5G)	sg.m2	PCIe2 (5/2.5)		sg.m4	sg.m5
0x88	PCIe1 (5/2.5)	sg.m3	sg.m1	sg.m2	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SATA.2 (3/1.5)	SATA.1 (3/1.5)
0xA5	PCIe1 (5/2.5)	sg.m3	sg.m1 (2.5G)	sg.m2 (2.5G)	PCIe2 (5/2.5)		sg.m4	sg.m5

This table shows SerDes assignments applicable to T1024 only and does not apply to T1022. For nomenclature, refer QorIQ T1024 Reference Manual.

SRDS_PRTCL_S1 (RCW[128:136])	SerDes Lanes			
	A	B	C	D
0x095	XFIa (MACa)	PCIec (5/2.5)	PCIeb (5/2.5)	PCIea (5/2.5)
0x0d5	QSGMIa (qs.ma-d)	PCIec (5/2.5)	PCIeb (5/2.5)	PCIea (5/2.5)
0xd6	QSGMIa (qs.ma-d)	PCIec (5/2.5)	PCIeb (5/2.5)	SATA.1 (3/1.5)
0x099	XFIa (MACa)	PCIec (5/2.5)	SGMII 1G (sg.mb 1G)	PCIea (5/2.5)
0x06B	PCIea (5/2.5)	SGMII 1G (sg.mc 1G)	SGMII 1G (sg.mb 1G)	SGMII 1G (sg.ma 1G)
0x06A	PCIea (5/2.5)	SGMII 1G (sg.mc 1G)	SGMII 1G (sg.mb 1G)	SATA.1 (3/1.5)
0x05A	PCIea (5/2.5)	PCIec (5/2.5)	SGMII 1G (sg.mb 1G)	SATA.1 (3/1.5)
0x119	Aurora	PCIec (5/2.5)	SGMII 1G (sg.mb 1G)	PCIea (5/2.5)
0x077	PCIea (5/2.5)	SGMII 2.5G (sg.mc 2.5G)	PCIeb (5/2.5)	SGMII 1G (sg.ma 1G)
0x135	Aurora	SGMII 2.5G (sg.mc 2.5G)	PCIeb (5/2.5)	PCIea (5/2.5)
0x05F	PCIea (5/2.5)	PCIec (5/2.5)	SGMII 2.5G (sg.mb 2.5G)	SGMII 2.5G (sg.ma 2.5G)

Figure 7. SerDes assignments applicable to T1024 only

This table shows the compatible SerDes configuratons between T1024 and T1022. For nomenclature, refer the respective Reference Manuals.

Table 7. T1024/T1022 SerDes Assignments compatibility

T1024 SRDS_PRCTL_S1 RCW[128:136]	A	B	C	D	E	F	G	H	T1022 SRDS_PRTCL_S1 RCW[128:135]
	NC	NC	NC	NC	A	B	C	D	
0x040	PCIe1 (5/2.5)				PCIe2 (5/2.5)				0x00
	PCIe1 (5/2.5)		sg.m1	sg.m2	PCIe2 (5/2.5)				0x40

Table continues on the next page...

Table 7. T1024/T1022 SerDes Assignments compatibility (continued)

T1024 SRDS_PRCTL_S1 RCW[128:136]	A	B	C	D	E	F	G	H	T1022 SRDS_PRTCL_S1 RCW[128:135]
	NC	NC	NC	NC	A	B	C	D	
	N/A	N/A	N/A	N/A	PCIea (5/2.5)[1]				
0x05B	PCIe1 (5/2.5)	sg.m3	sg.m1 (2.5G)	sg.m2 (2.5G)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	sg.m4 1G	sg.m5 1G	0xAA
	N/A	N/A	N/A	N/A	PCIea (5/2.5)	PCIec (5/2.5)	sg.mb 1G	sg.ma 1G	
0x046	PCIe1 (5/2.5)	sg.m3	sg.m1	sg.m2	PCIe2 (5/2.5)		PCIe4 (5/2.5)	SATA.1 (3/1.5)	0x81
	N/A	N/A	N/A	N/A	PCIea (5/2.5)		PCIeb (5/2.5)	SATA.1 (3/1.5)	

1. In T1024, PCI Express link width equal to x4 is only supported by PCIe Gen 1. T1024 does not support link width equal to x4 in PCIe Gen 2 mode.

4.10.2 Compatible SerDes option for 2.5G SGMII

The table shows the use of 2.5G SGMII for common board design between T1024 and T1022.

T1024 SRDS_PRCTL_S1 RCW [128:136]	A	B	C	D	E	F	G	H	T1022 SRDS_PRTCL_S1 RCW [128:135]
	NC	NC	NC	NC	A	B	C	D	
	PCIe1 (5/2.5)	sg.m3	sg.m1 (2.5G)	sg.m2 (2.5G)	PCIe2 (5/2.5)	PCIe2 (5/2.5)	PCIe4 (5/2.5)	sg.m5	0xA7
0x077	N/A	N/A	N/A		PCIea (5/2.5)	sg.mc (2.5G)	PCIeb (5/2.5)	sg.ma (1G)	

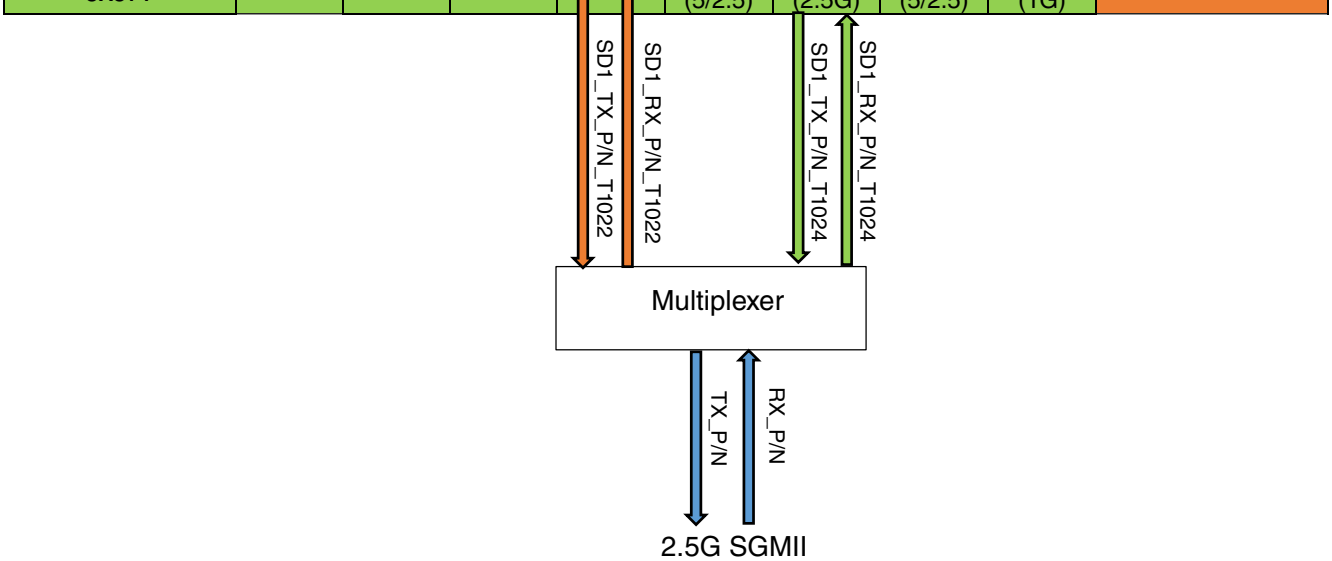

Figure 8. T1024 and T1022 SerDes option for 2.5G SGMII

The multiplexer should select lane-D of T1022 when T1022 is mounted and it should select Lane-B of T1024.

when T1024 is mounted. Ensure the quality of differential signals remain intact at the outputs of multiplexer.

NOTE

1. Similar implementation can be applied for choosing between lane-C of T1022 and lane-B of T1024
2. The same implementation can be applied for other SerDes options

Alternatively, the multiplexer can be replaced using optional resistors and capacitors as given in Figure 9 and Figure 10. The following figure shows the connection diagram when T1022 is mounted.

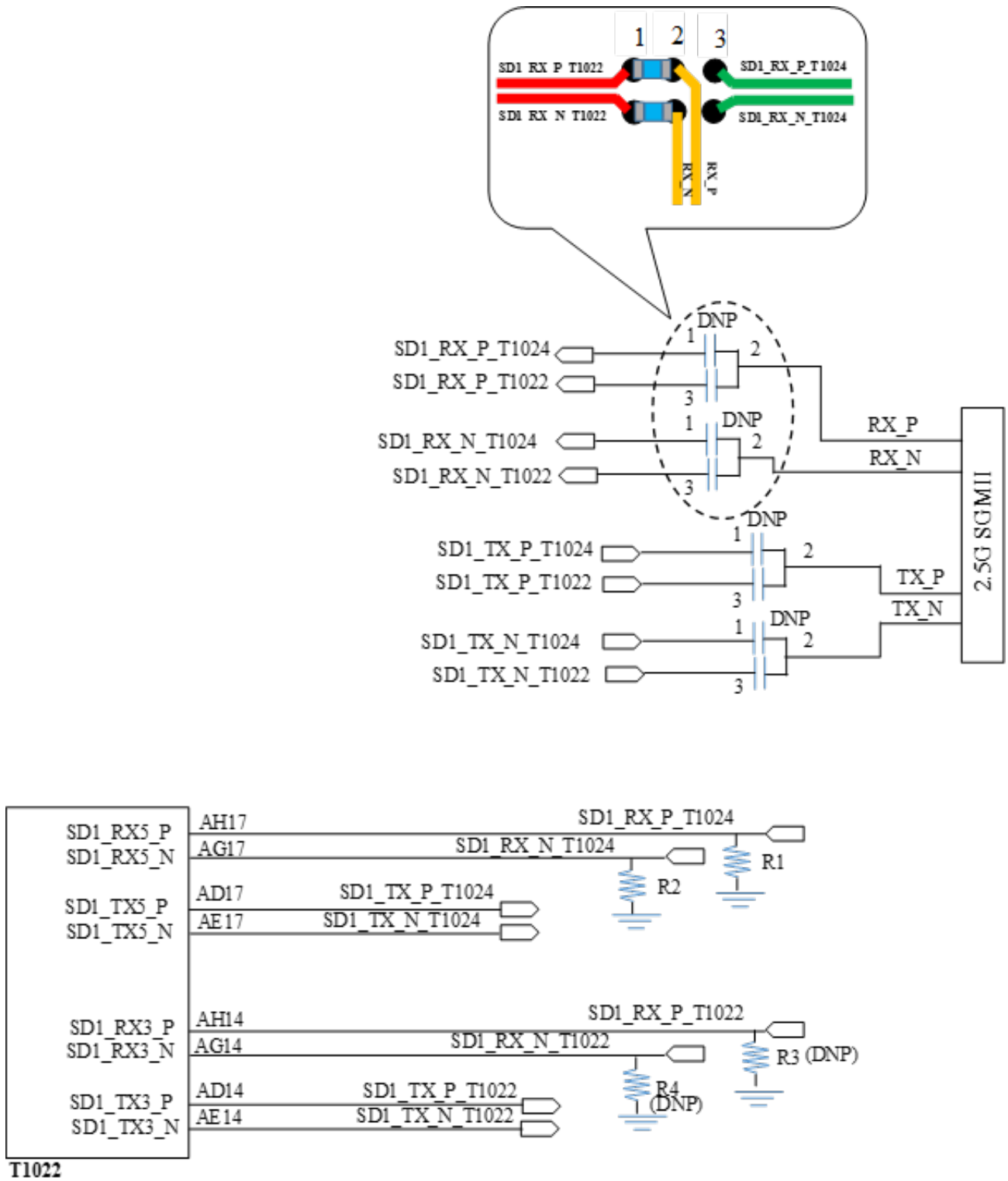

Figure 9. Common board design for 2.5G SGMII using T1022

In the figure above, DNP denotes “Do Not Populate” the component.

The following figure shows the connection diagram when T1024 is mounted.

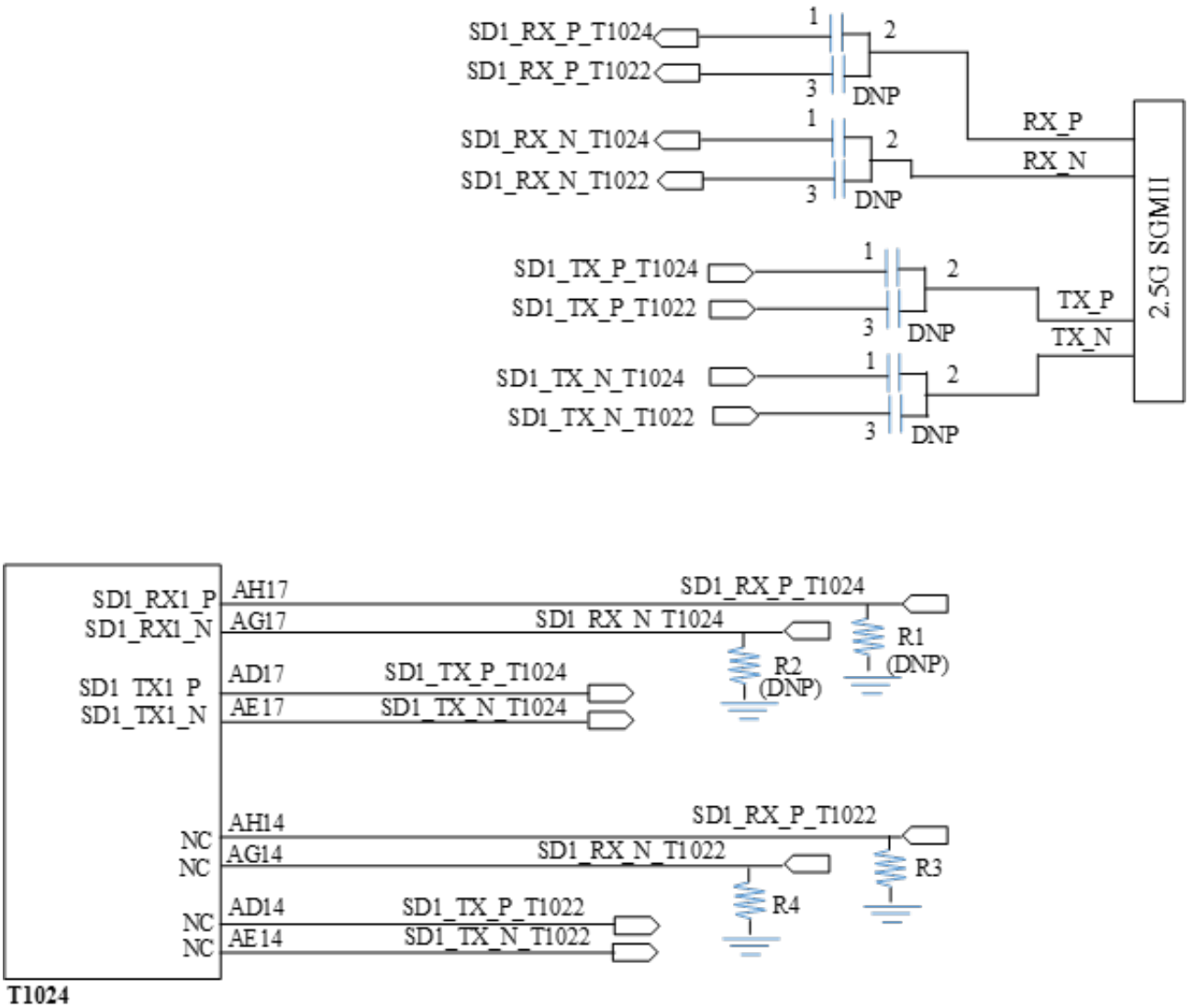

Figure 10. Common board design for 2.5G SGMII using T1024

NOTE

1. SerDes lanes must be powered down when not in use
2. PCB layout should not introduce stubs on differential pairs.

4.11 Ethernet MACs options

While the two RGMII interfaces are pin compatible, the configurations for RGMII mode are different between T1024 and T1022 devices. This table lists the RGMII configuration options and the assigned FMan/MACx on both T1024 and T1022.

Table 8. Configuration for RGMII mode

Configuration	RGMII assignment		
	T1024	T1022	
RCW[EC1] = 0b00	FMan MAC1	FMan MAC4	MAC2_GMII_SEL = 0b0

Table continues on the next page...

Table 8. Configuration for RGMII mode (continued)

		FMan MAC2	MAC2_GMII_SEL = 0b1
RCW[EC2] = 0b00	-	FMan MAC5	-
RCW[EC2] = 0b10	FMan MAC2	-	

T1022 also supports MII on EC1 which is not supported on T1024. It is recommended not to use MII mode on common board design.

4.12 Power management recommendations

For supporting this feature, power rails have been categorized into Always ON and switchable category and need separate planes on board.

4.13 Power island requirements

T1024 has different power islands when compared to T1022.

4.13.1 Core power island

V_{DD} and V_{DDC} are identical between T1024 and T1022.

4.13.2 I/O power island requirements

The table summarizes the Power island requirements for T1024 and T1022 and provides recommendations for common board design.

Table 9. I/O Power island configuration

Supply	T1024	T1022	Recommendation for a common board design	Interfaces
$O1V_{DD}$	1.8 V	1.8 V	Identical	IRQ[0],IRQ[1], System Control, ASLEEP, SYSCLK, DIFF_SYSCLK, EVT[0-4], PCKG_SEL.
OV_{DD}	1.8 V	1.8 V		IFC, RTC, DDRCLK, Trust, CKSTP_OUT_B, JTAG, GPIO2
DV_{DD}	3.3 V 2.5 V 1.8 V	3.3 V 2.5 V 1.8 V	Identical	DUART, I2C, QE-TDM, IRQ[5], DIU T1022: DMA,
CV_{DD}	3.3 V 1.8 V	3.3 V 1.8 V	Identical	eSPI, IRQ[4], eSDHC (Card Detect and Write Protect, SDHC[4:7])
EV_{DD}	3.3 V 1.8 V	3.3 V 1.8 V	Identical	eSDHC[0:3], SDHC_CLK, SDHC_CMD
$G1V_{DD}$	1.35 V	1.35 V	Identical	DDR3L/ DDR4

Table continues on the next page...

Table 9. I/O Power island configuration (continued)

Supply	T1024	T1022	Recommendation for a common board design	Interfaces
	1.2 V	1.2 V		
$L1V_{DD}$	2.5 V 1.8 V	3.3 V 2.5 V 1.8 V	No MII support in T1024 Use RGMII interface at 2.5 V/ 1.8 V	IRQ2, IRQ3, EC1 Ethernet management, GPIO3(8:23)
LV_{DD}	2.5 V 1.8 V	3.3 V 2.5 V 1.8 V	Use RGMII interface at 2.5 V/ 1.8 V	IEEE1588, EC2, GPIO3(0:7)
TV_{DD}	1.2 V	N/A	When EMI 2 is used, connect TVDD to 1.2V power supply. When EMI 2 is not used, TVDD must remain powered to 1.2V or 1.8V (OVDD).	MDIO interface for 10G FMAN (Ethernet management interface 2)

4.14 Power sequencing requirements

T1024 and T1022 have same power sequence requirements.

4.15 TEST_SEL_B requirements

When migrating between T1024 and T1022, the connection of TEST_SEL_B needs to be considered. This table lists the different TEST_SEL_B connection requirements for each chip.

Table 10. TEST_SEL_B pin connection requirements

Device	TEST_SEL_B pin requirement
T1024	Pull to O1VDD through 100-ohm to 1K-ohm resistor
T1014	Pull to GND
T1042	Pull to O1VDD through 100-ohm to 1K-ohm resistor
T1022	Pull to GND

4.16 MPIC requirements

When migrating between T1024 and T1022, the connection of IRQ lines need to be considered.

- T1024 supports IRQ[0:5] whereas T1022 supports IRQ[0:11]
- These IRQ lines are mapped on different balls between T1024 and T1022, see Table 13

This table lists the differences between the IRQ lines.

Table 11. T1024 and T1022 IRQ voltage compatibility

Voltage	T1024	T1022	Pin#
$O1V_{DD}$	IRQ[0]	IRQ[0]	F7
	IRQ[1]	IRQ[1]	D3
	IRQ_OUT_B	IRQ_OUT_B	A3
	NC	IRQ[2:5]	E9, D1, D4, D5
$L1V_{DD}$	IRQ[2]	IRQ[6]	AB4
	IRQ[3]	IRQ[9]	AC5
	NC	IRQ[7:8]	AD5, AB1
CV_{DD}	IRQ4	IRQ10	L4
DV_{DD}	IRQ5	IRQ11	D5

5 Internal clocking differences

T1024 supports additional clocking schemes and differences are summarized in the table below.

Table 12. T1022/T1024 clocking comparison

Clocking scheme	T1024	T1022	Recommendation
Single Reference clock mode	Yes	Yes	DIFF_SYSCLK/DIFF_SYSCLK_B clock input pair. Recommended mode for common board design.
Multiple reference clock mode	Yes	Yes	Through separate oscillators for SYSCLK, DDRCLK, USBCLK, SDREF_CLKn inputs. Also refer USB controller recommendation" , for difference in USBCLK.

NOTE

For a common board design, use Single reference clock mode and connect SYSCLK, DDRCLK inputs to ground.

6 Pinout comparison

This table details the differences in pinout between T1024 and T1022 processor family and how to resolve this difference. Unless explicitly stated otherwise, the pins on T1022 can be connected as if a T1024 is populated.

Table 13. T1024 to T1022 pinout comparison

Pin	T1024	T1022	Compatible connection
Integrated Flash Controller			
E17	NC	IFC_CS4_B/ GPIO1_09	All unused outputs can be left floating.
C17	NC	IFC_CS5_B/ GPIO1_10	
D18	NC	IFC_CS6_B/ GPIO1_11	

Table continues on the next page...

Table 13. T1024 to T1022 pinout comparison (continued)

Pin	T1024	T1022	Compatible connection
C19	NC	IFC_CS7_B/ GPIO1_12	Alternatively, signals can be configured as GPIO through RCW bits, configure them as output only and leave floating.
C10	IFC_A25/ GPIO2_25/ IFC_WP1_B/ IFC_CS4_B	IFC_A25/ GPIO2_25/ IFC_WP1_B	All unused outputs can be left floating. Alternatively, signals can be configured as GPIO through RCW bits, configure them as output only and leave floating. To use these signals for IFC, refer IFC recommendations"
E11	IFC_A26/ GPIO2_26/ IFC_WP2_B/ IFC_CS5_B	IFC_A26/ GPIO2_26/ IFC_WP2_B	
C11	IFC_A27/ GPIO2_27/ IFC_WP3_B/ IFC_CS6_B	IFC_A27/ GPIO2_27/ IFC_WP3_B	
USB			
F8	NC	USBCLK	To use these signals for USB, refer USB controller recommendation" Alternatively, IRQ1 can be used on common board design.
D3	IRQ1/ USBCLK/ SDHC_VS	IRQ01	
Ethernet Management Interface 2			
U6	EMI2_MDC	NC11	All Ethernet PHY's to be used with T1022 should be managed through EMI1 interface.
V6	EMI2_MDIO	NC12	
Ethernet Controller 1			
AC1	NC	EC1_COL/ GPIO3_10/ MII_COL/ MAC2_MII_COL	Tie to GND through 2k-10K resistor, if not used.
AC2	NC	EC1_RX_ER/ GPIO3_09/ MII_RX_ER/ MAC2_MII_RX_ER	
AC4	NC	EC1_TX_ER/ GPIO3_08/ MII_TX_ER/ MAC2_MII_TX_ER	This output pin can be left floating if not used.
Ethernet Controller 2			
AC6	GPIO3_26/ EC2_TXD3	EC2_GTX_CLK125/ GPIO4_29	All inputs should be tied to GND through 2K-10K resister, if not used. All unused outputs can be left floating. Alternatively, signals can be configured as GPIO through RCW bits, configure them as output only and leave floating.
AE7	NC	EC2_TXD0/ GPIO3_27	
AE8	GPIO3_25/ EC2_RXD0	EC2_GTX_CLK/ GPIO4_28	
AF6	NC	EC2_TXD2/ GPIO3_25	
AF7	NC	EC2_TXD1/ GPIO3_26	
AF8	GPIO3_24/ EC2_RX_DV	EC2_TX_CTL/ GPIO4_27	
AG5	NC	EC2_TXD3/ GPIO3_24	
AG7	NC	EC2_RXD1/ GPIO3_30	
AG8	NC	EC2_RX_CTL/ GPIO4_30	
AH5	NC	EC2_RX_CLK/ GPIO4_31	
AH6	GPIO3_27/ EC2_RXD3	EC2_RXD3/ GPIO3_28	
AH7	GPIO3_28/ EC2_RXD1	EC2_RXD2/ GPIO3_29	
AH8	NC	EC2_RXD0/ GPIO3_31	
AF5	TSEC_1588_ALARM_OUT1/ GPIO3_03/ EC2_RX_CLK	TSEC_1588_ALARM_OUT1/ GPIO3_03	Only TSEC_1588 or GPIOs are recommended to be used on common board design.

Table continues on the next page...

Table 13. T1024 to T1022 pinout comparison (continued)

Pin	T1024	T1022	Compatible connection
AC7	TSEC_1588_ALARM_OUT 2/ GPIO3_04/ EC2_TXD0	TSEC_1588_ALARM_OUT2/ GPIO3_04/EMI1_MDC	
AC8	TSEC_1588_CLK_IN/ GPIO3_00/ EC2_GTX_CLK	TSEC_1588_CLK_IN/ GPIO3_00	
AD7	TSEC_1588_CLK_OUT/ GPIO3_05/ EC2_TXD1	TSEC_1588_CLK_OUT/ GPIO3_05	
AE6	TSEC_1588_PULSE_OUT1 / GPIO3_06/ EC2_RXD2	TSEC_1588_PULSE_OUT1/ GPIO3_06	
AD8	TSEC_1588_PULSE_OUT2 / GPIO3_07/ EC2_TX_EN	TSEC_1588_PULSE_OUT2/ GPIO3_07	
AB6	TSEC_1588_TRIG_IN1/ GPIO3_01/ EC2_TXD2	TSEC_1588_TRIG_IN1/ GPIO3_01	
AE5	TSEC_1588_TRIG_IN2/ GPIO3_02/ EC2_GTX_CLK125	TSEC_1588_TRIG_IN2/ GPIO3_02/EMI1_MDIO	
SerDes			
AD10	NC	SD1_TX0_P	These pins should be left floating, if not used.
AD11	NC	SD1_TX1_P	
AD13	NC	SD1_TX2_P	
AD14	NC	SD1_TX3_P	
AD16	SD1_TX0_P	SD1_TX4_P	Use these pins as recommended in SerDes recommendations"
AD17	SD1_TX1_P	SD1_TX5_P	
AD19	SD1_TX2_P	SD1_TX6_P	
AD20	SD1_TX3_P	SD1_TX7_P	
AE10	NC	SD1_TX0_N	These pins should be left floating, if not used.
AE11	NC	SD1_TX1_N	
AE13	NC	SD1_TX2_N	
AE14	NC	SD1_TX3_N	
AE16	SD1_TX0_N	SD1_TX4_N	Use these pins as recommended in SerDes recommendations".
AE17	SD1_TX1_N	SD1_TX5_N	
AE19	SD1_TX2_N	SD1_TX6_N	
AE20	SD1_TX3_N	SD1_TX7_N	
AG10	NC	SD1_RX0_N	These pins should be connected to S1GND if not used.
AG11	NC	SD1_RX1_N	
AG13	NC	SD1_RX2_N	
AG14	NC	SD1_RX3_N	
AG16	SD1_RX0_N	SD1_RX4_N	Use these pins as recommended in SerDes recommendations"
AG17	SD1_RX1_N	SD1_RX5_N	
AG19	SD1_RX2_N	SD1_RX6_N	
AG20	SD1_RX3_N	SD1_RX7_N	
AH10	NC	SD1_RX0_P	These pins should be connected to S1GND if not used.
AH11	NC	SD1_RX1_P	

Table continues on the next page...

Table 13. T1024 to T1022 pinout comparison (continued)

Pin	T1024	T1022	Compatible connection
AH13	NC	SD1_RX2_P	
AH14	NC	SD1_RX3_P	
AH16	SD1_RX0_P	SD1_RX4_P	Use these pins as recommended in SerDes recommendations"
AH17	SD1_RX1_P	SD1_RX5_P	
AH19	SD1_RX2_P	SD1_RX6_P	
AH20	SD1_RX3_P	SD1_RX7_P	
IRQ			
D1	NC	IRQ03/ GPIO1_23/ SDHC_VS	Connect IRQ to respective supplies bank through 2K-10K resistor. Refer MPIC requirements" for supply bank. Alternatively, configure these pin as GPIO, configure as output and leave floating.
D4	NC	IRQ04/ GPIO1_24	
D5	NC	IRQ05/ GPIO1_25	
E9	NC	IRQ02	
L4	IRQ4/ GPIO1_24/ SDHC_CLK_SYNC_IN	IRQ10/ GPIO1_30/ SDHC_CLK_SYNC_IN	
U3	IRQ5/ GPIO1_25	IRQ11/ GPIO1_31	
AB1	NC	IRQ08/ GPIO1_28	
AB4	IRQ2	IRQ06/ GPIO1_26	
AC5	IRQ3/ GPIO1_23	IRQ09/ GPIO1_29	
AD5	NC	IRQ07/ GPIO1_27	
DMA			
P5	NC	DMA1_DREQ0_B/ GPIO4_04/ TDM_TXD	All inputs should be tied to GND through 2K-10K resister, if not used. All unused outputs can be left floating. Alternatively, signals can be configured as GPIO through RCW bits, configure them as output only and leave floating.
R5	NC	DMA1_DDONE0_B/ GPIO4_06/ TDM_TCK	
U5	NC	DMA1_DACK0_B/ GPIO4_05/ TDM_TFS	
V5	NC	DMA2_DREQ0_B/ GPIO4_07/ TDM_RXD	
Y5	NC	DMA2_DDONE0_B/ GPIO4_09/ EVT8_B/ TDM_RCK	
AA5	NC	DMA2_DACK0_B/ GPIO4_08/ EVT7_B/ TDM_RFS	
K3	SDHC_CMD/ GPIO2_04/ DMA1_DREQ0_B	SDHC_CMD/ GPIO2_04	On common board design, SDHC is recommended to be used on these pins. Refer eSDHC recommendation for more details.
L2	SDHC_DAT0/ GPIO2_05/ DMA1_DACK0_B	SDHC_DAT0/ GPIO2_05	
K4	SDHC_DAT1/ GPIO2_06/ DMA1_DDONE0_B	SDHC_DAT1/ GPIO2_06	
L3	SDHC_DAT2/ GPIO2_07/ DMA2_DREQ0_B	SDHC_DAT2/ GPIO2_07	
L1	SDHC_DAT3/ GPIO2_08/ DMA2_DACK0_B	SDHC_DAT3/ GPIO2_08	
K1	SDHC_CLK/ GPIO2_09/ DMA2_DDONE0_B	SDHC_CLK/ GPIO2_09	

Table continues on the next page...

Table 13. T1024 to T1022 pinout comparison (continued)

Pin	T1024	T1022	Compatible connection
I2C			
V2	NC	IIC3_SCL/ GPIO4_00	
W3	NC	IIC3_SDA/ GPIO4_01	
L5	SDHC_CD_B/ GPIO4_24/ IIC3_SCL	SDHC_CD_B/ GPIO4_24	
M5	SDHC_WP/ GPIO4_25/ IIC3_SDA	SDHC_WP/ GPIO4_25	
V3	IIC2_SCL/ GPIO4_27	IIC2_SCL	Use these pins for IIC2 on common board design.
Y3	IIC2_SDA/ GPIO4_28	IIC2_SDA	
Power and ground pins			
G12	NC	AVDD_CGA2	On common board design, connect all NC pins of T1024 as perT1022 power supply or ground.
AC9	NC	X1VDD1	
AC12	X1VDD1	X1VDD2	
AC15	X1VDD2	X1VDD3	
AC18	X1VDD3	X1VDD4	
AC21	X1VDD4	X1VDD5	
AC10	NC	X1GND01	
AC11	NC	X1GND02	
AC13	SD_GND15	X1GND03	
AC14	SD_GND16	X1GND04	
AC16	SD_GND17	X1GND05	
AC17	SD_GND18	X1GND06	
AC19	SD_GND19	X1GND07	
AC20	SD_GND20	X1GND08	
AD9	NC	X1GND09	
AD12	NC	X1GND10	
AD15	SD_GND21	X1GND11	
AD18	SD_GND22	X1GND12	
AD21	SD_GND23	X1GND13	
AE9	NC	X1GND14	
AE12	NC	X1GND15	
AE15	SD_GND24	X1GND16	
AE18	SD_GND25	X1GND17	
AE21	SD_GND26	X1GND18	
AF10	NC	S1GND13	
AF11	NC	S1GND14	
AF12	NC	S1GND15	
AF13	NC	S1GND16	
AF14	NC	S1GND17	On common board design, connect all NC pins of T1024 as per T1022 power supply or ground.
AF15	SD_GND27	S1GND18	

Table continues on the next page...

Table 13. T1024 to T1022 pinout comparison (continued)

Pin	T1024	T1022	Compatible connection
AF16	SD_GND28	S1GND19	
AF17	SD_GND29	S1GND20	
AF18	SD_GND30	S1GND21	
AF19	SD_GND31	S1GND22	
AF20	SD_GND32	S1GND23	
AG9	NC	S1GND24	
AG12	NC	S1GND25	
AG15	SD_GND33	S1GND26	
AG18	SD_GND34	S1GND27	
AG21	SD_GND35	S1GND28	
AH9	NC	S1GND29	
AH12	NC	S1GND30	
AH15	SD_GND36	S1GND31	
AH18	SD_GND37	S1GND32	
AH21	SD_GND38	S1GND33	
AA7	GND148	NC20	
L20	NC	VDD	
M19	NC	VDD	
N20	NC	VDD	
P19	NC	VDD	
R20	NC	VDD	
T19	NC	VDD	
U20	NC	VDD	
V19	NC	VDD	
W14	NC	VDD	
T6	TVDD	NC09	When EMI 2 is used, connect TVDD to 1.2V power supply. When EMI 2 is not used, TVDD must remain powered to 1.2V or 1.8V (OVDD).

7 Related documentation

The following documents must be referred to when considering T1024 and T1022 chips. Contact your NXP sales representative for access to any documents that are not publicly available on the NXP website.

- *QorIQ T1024 Reference Manual*
- *QorIQ T1040 Reference Manual*
- *QorIQ T1024, T1014 Datasheet*
- *QorIQ T1042, T1022 Datasheet*
- *T1024, T1014, T1023, and T1013 Chip Errata*

- *T1040 Chip Errata*
- *PowerPC e5500 Core Reference Manual*

8 Revision history

This table summarizes changes to this document.

Table 14. Document revision history

Rev. number	Date	Substantive Change(s)
0	07/2017	Initial release

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number AN4829
Revision 0, 07/2017