

NTS0102

Dual supply translating transceiver; open-drain; auto direction sensing

Rev. 4.5 — 6 July 2023

Product data sheet

1 General description

The NTS0102 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.65 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 2.3 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V, and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range:
 - $V_{CC(A)}$: 1.65 V to 3.6 V and $V_{CC(B)}$: 2.3 V to 5.5 V
- Maximum data rates:
 - Push-pull: 50 Mbit/s
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
 - HBM JESD22-A114E Class 2 exceeds 2500 V for A port
 - HBM JESD22-A114E Class 3B exceeds 8000 V for B port
 - CDM JESD22-C101E exceeds 1500 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3 Applications

- $I^2\text{C}/\text{SMBus}$
- UART
- GPIO

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NTS0102DP	s02	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2



Dual supply translating transceiver; open-drain; auto direction sensing

Table 1. Ordering information...continued

Type number	Topside marking	Package		
		Name	Description	Version
NTS0102GT	s02	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
NTS0102GD	s02	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2
NTS0102GF	s2	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
NTS0102TL	ts2	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT1052-2
NTS0102JK	s2	X2SON8	super thin small outline; no leads, 8 terminals, 0.35 mm pitch, 1.35 mm x 1 mm x 0.32 mm body	SOT2015-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method ^[1]	Minimum order quantity	Temperature
NTS0102DP	NTS0102DP,125	TSSOP8	Reel 7" Q3 NDP	3000	−40 °C to +125 °C
NTS0102GT	NTS0102GT,115	XSON8	Reel 7" Q1 NDP	5000	−40 °C to +125 °C
NTS0102GD ^[2]	NTS0102GD,125	XSON8	Reel 7" Q3 NDP	3000	−40 °C to +125 °C
NTS0102GF	NTS0102GF,115	XSON8	Reel 7" Q1 NDP	5000	−40 °C to +125 °C
NTS0102TL	NTS0102TLH	XSON8	Reel 7" Q3 NDP	4000	−40 °C to +125 °C
NTS0102JK	NTS0102JKZ	X2SON8	Reel 7" Q1 NDP SSB	6000	−40 °C to +125 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

[2] Discontinuation Notice 202111012DN - drop in replacement is NTS0102TLH.

The TL package has a center pad vs no center pad for the GD package. The TL package pad is not electrically connected to the silicon and is not required to connect to the PCB so it can drop onto the GD package PCB layout. If the existing GD package has a trace underneath the risk is low since the TL package center pad is not connected to the silicon. If there are multiple traces there could be EMI and cross talk. In both cases the customer needs to evaluate risk.

Note: The length and width are reversed between the "GD" and "TL" package drawings but the shorter edge contains the pins and is 2.0 mm in both cases.

5 Functional diagram

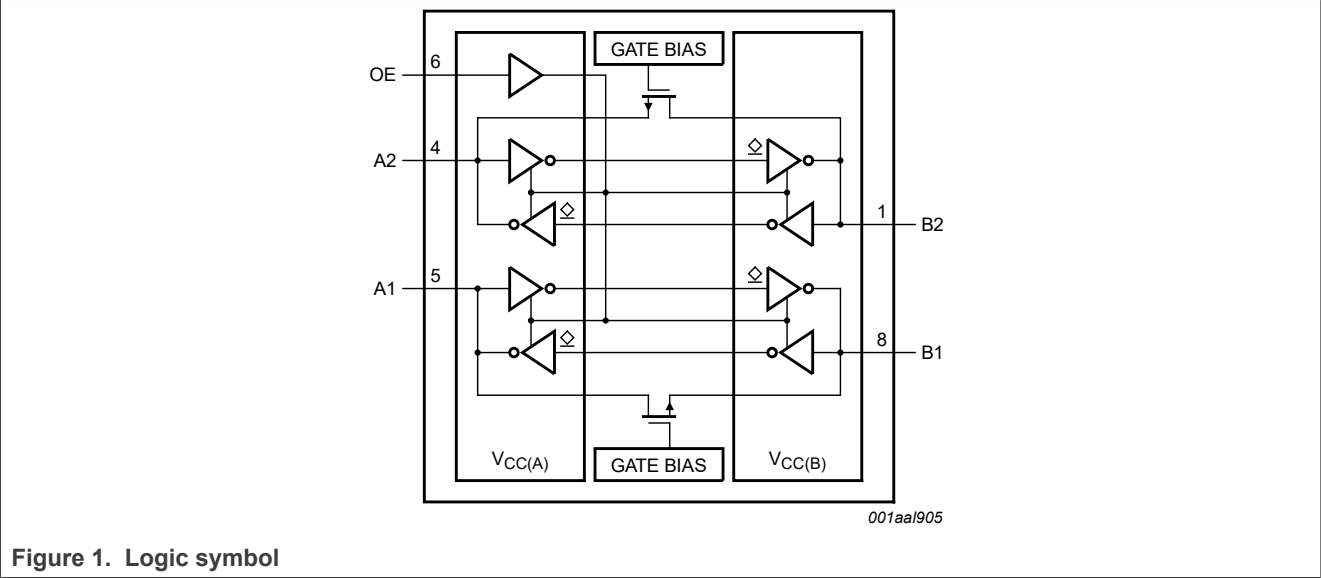


Figure 1. Logic symbol

6 Pinning information

6.1 Pinning

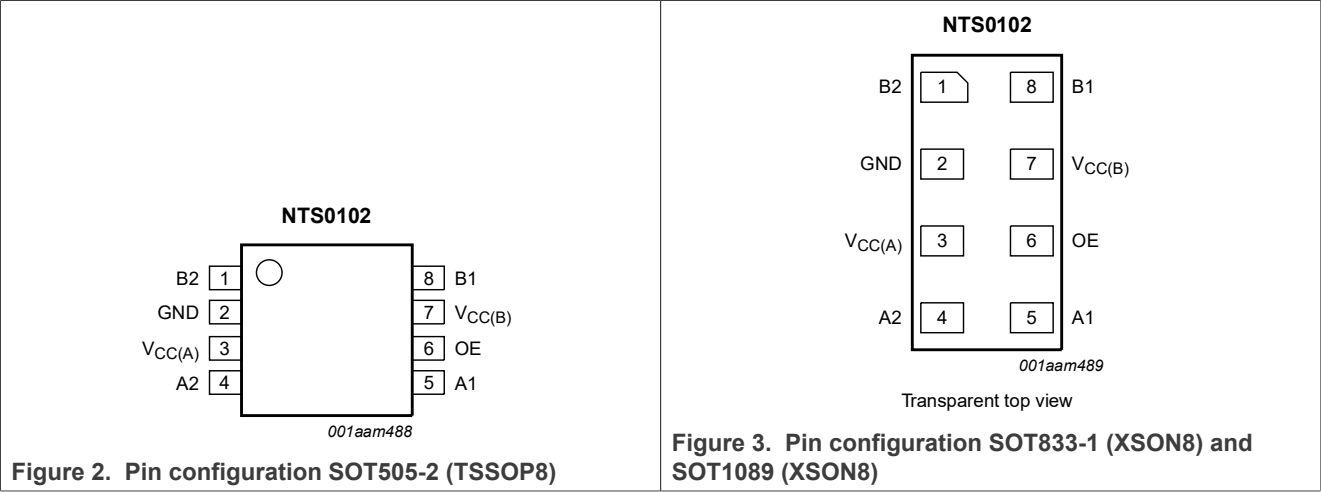
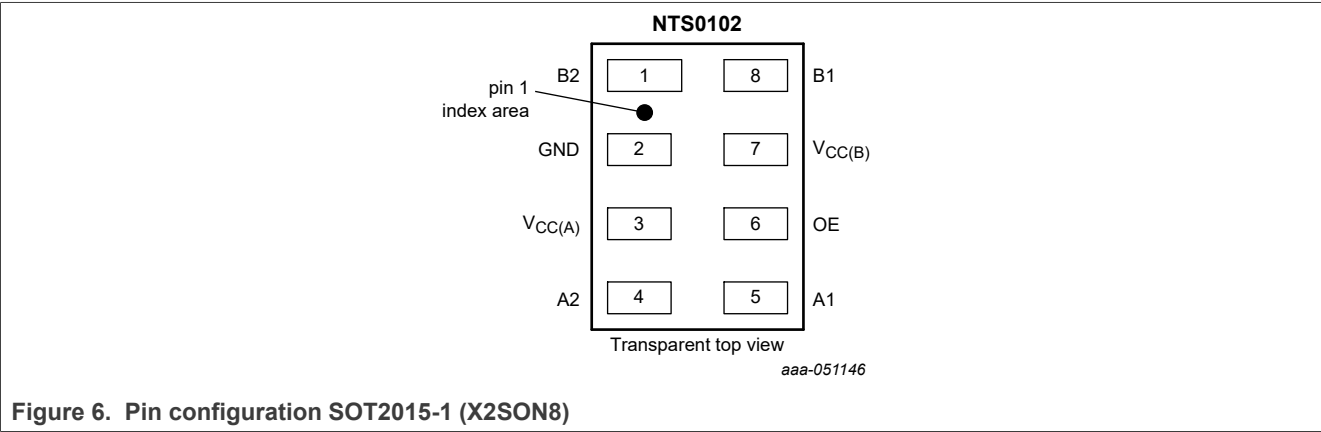
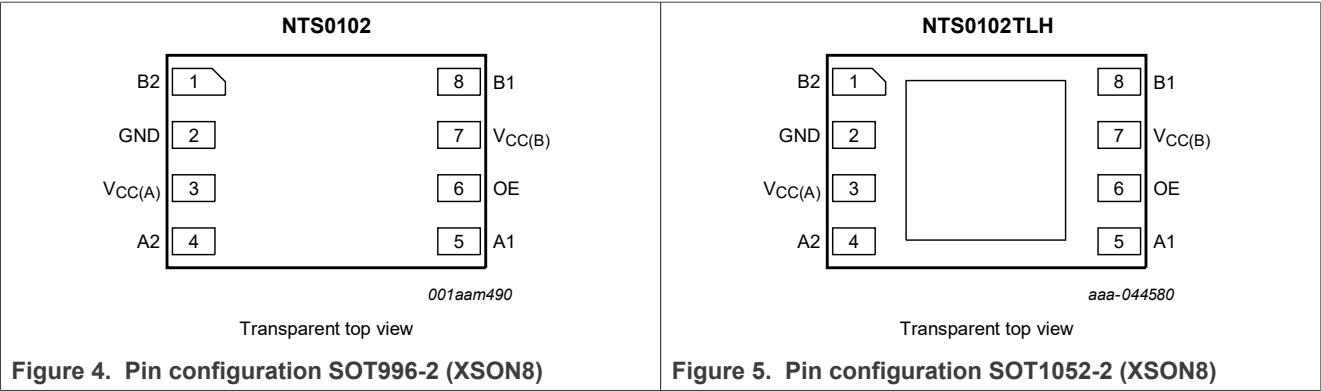


Figure 2. Pin configuration SOT505-2 (TSSOP8)

Figure 3. Pin configuration SOT833-1 (XSON8) and SOT1089 (XSON8)



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B2, B1	1, 8	data input or output (referenced to $V_{CC(B)}$)
GND	2	ground (0 V)
$V_{CC(A)}$	3	supply voltage A
A2, A1	4, 5	data input or output (referenced to $V_{CC(A)}$)
OE	6	output enable input (active HIGH; referenced to $V_{CC(A)}$)
$V_{CC(B)}$	7	supply voltage B

7 Functional description

Table 4. Function table^[1]

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	L	Z	Z
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	H	input or output	output or input
GND ^[2]	GND ^[2]	X	Z	Z

Dual supply translating transceiver; open-drain; auto direction sensing

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
V_I	input voltage	A port and OE input [1] [2]	-0.5	+6.5	V
		B port [1] [2]	-0.5	+6.5	V
V_O	output voltage	Active mode [1] [2]			
		A or B port	-0.5	$V_{CCO} + 0.5$	V
		Power-down or 3-state mode [1]			
		A port	-0.5	+4.6	V
		B port	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	—	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	—	mA
I_O	output current	$V_O = 0$ V to V_{CCO} [2]	—	± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	—	100	mA
I_{GND}	ground current		-100	—	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]	—	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

[3] For TSSOP8 package: above 55 °C, the value of P_{tot} derates linearly with 2.5 mW/K.
For XSON8 packages: above 118 °C, the value of P_{tot} derates linearly with 7.8 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions^{[1][2]}

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	—	10	ns/V
		OE input			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	—	10	ns/V

Dual supply translating transceiver; open-drain; auto direction sensing

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

10 Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}$; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	—	—	± 1	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}$; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ ^[1]	—	—	± 1	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V to }3.6\text{ V}$; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	—	—	± 1	μA
		B port; V_I or $V_O = 0\text{ V to }5.5\text{ V}$; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	—	—	± 1	μA
C_I	input capacitance	OE input; $V_{CC(A)} = 3.3\text{ V}$; $V_{CC(B)} = 3.3\text{ V}$	—	1	—	pF
$C_{I/O}$	input/output capacitance	A port	—	5	—	pF
		B port	—	8.5	—	pF
		A or B port; $V_{CC(A)} = 3.3\text{ V}$; $V_{CC(B)} = 3.3\text{ V}$	—	11	—	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

V _{CC(A)}	V _{CC(B)}						Unit
	2.5 V		3.3 V		5.0 V		
	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	μA
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	μA
3.3 V	—	—	0.1	0.1	0.1	2.8	μA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port					
		$V_{CC(A)} = 1.65\text{ V to }1.95\text{ V}$; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ ^[1]	$V_{CCI} - 0.2$	—	$V_{CCI} - 0.2$	—	V
		$V_{CC(A)} = 2.3\text{ V to }3.6\text{ V}$; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$ ^[1]	$V_{CCI} - 0.4$	—	$V_{CCI} - 0.4$	—	V

Dual supply translating transceiver; open-drain; auto direction sensing

Table 9. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
		B port					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$ ^[1]	$V_{CCI} - 0.4$	—	$V_{CCI} - 0.4$	—	V
		OE input					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	$0.65V_{CC(A)}$	—	$0.65V_{CC(A)}$	—	V
V_{IL}	LOW-level input voltage	A or B port					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	0.15	—	0.15	V
		OE input					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	$0.35V_{CC(A)}$	—	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	$I_O = -20 \mu\text{A}$					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$ ^[2]	$0.67V_{CCO}$	—	$0.67V_{CCO}$	—	V
V_{OL}	LOW-level output voltage	A or B port; $I_O = 1 \text{ mA}$ ^[2]					
		$V_I \leq 0.15 \text{ V}; V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	0.4	—	0.4	V
I_I	input leakage current	OE input; $V_I = 0 \text{ V to } 3.6 \text{ V}; V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	± 2	—	± 12	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0 \text{ V or } V_{CCO}; V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$ ^[2]	—	± 2	—	± 12	μA
I_{OFF}	power-off leakage current	A port; $V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 0 \text{ V to } 5.5 \text{ V}$	—	± 2	—	± 12	μA
		B port; $V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 0 \text{ V}; V_{CC(A)} = 0 \text{ V to } 3.6 \text{ V}$	—	± 2	—	± 12	μA
I_{CC}	supply current	$V_I = 0 \text{ V or } V_{CCI}; I_O = 0 \text{ A}$ ^[1]					
		$I_{CC(A)}$					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	2.4	—	15	μA
		$V_{CC(A)} = 3.6 \text{ V}; V_{CC(B)} = 0 \text{ V}$	—	2.2	—	15	μA
		$V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 5.5 \text{ V}$	—	-1	—	-8	μA
		$I_{CC(B)}$					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	12	—	30	μA
		$V_{CC(A)} = 3.6 \text{ V}; V_{CC(B)} = 0 \text{ V}$	—	-1	—	-5	μA
		$V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 5.5 \text{ V}$	—	1	—	6	μA

Dual supply translating transceiver; open-drain; auto direction sensing

Table 9. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
		$I_{CC(A)} + I_{CC(B)}$					
		$V_{CC(A)} = 1.65 \text{ V to } 3.6 \text{ V}; V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	—	14.4	—	30	μA

[1] V_{CCI} is the supply voltage associated with the input.[2] V_{CCO} is the supply voltage associated with the output.

11 Dynamic characteristics

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C^[1]Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.8 V ± 0.15 V									
t _{PHL}	HIGH to LOW propagation delay	A to B	—	4.6	—	4.7	—	5.8	ns
t _{PLH}	LOW to HIGH propagation delay	A to B	—	6.8	—	6.8	—	7.0	ns
t _{PHL}	HIGH to LOW propagation delay	B to A	—	4.4	—	4.5	—	4.7	ns
t _{PLH}	LOW to HIGH propagation delay	B to A	—	5.3	—	4.5	—	0.5	ns
t _{en}	enable time	OE to A; B	—	200	—	200	—	200	ns
t _{dis}	disable time	OE to A; no external load ^[2]	—	25	—	25	—	25	ns
		OE to B; no external load ^[2]	—	25	—	25	—	25	ns
		OE to A	—	230	—	230	—	230	ns
		OE to B	—	200	—	200	—	200	ns
t _{TLH}	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
t _{THL}	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.5	2.8	10.0	ns
t _{sk(o)}	output skew time	between channels ^[3]	—	0.7	—	0.7	—	0.7	ns
t _W	pulse width	data inputs	20	—	20	—	20	—	ns
f _{data}	data rate		—	50	—	50	—	50	Mbit/s
V _{CC(A)} = 2.5 V ± 0.2 V									
t _{PHL}	HIGH to LOW propagation delay	A to B	—	3.2	—	3.3	—	3.4	ns

Dual supply translating transceiver; open-drain; auto direction sensing

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	A to B	—	3.5	—	4.1	—	4.4	ns
t _{PHL}	HIGH to LOW propagation delay	B to A	—	3.0	—	3.6	—	4.3	ns
t _{PLH}	LOW to HIGH propagation delay	B to A	—	2.5	—	1.6	—	0.7	ns
t _{en}	enable time	OE to A; B	—	200	—	200	—	200	ns
t _{dis}	disable time	OE to A; no external load ^[2]	—	20	—	20	—	20	ns
		OE to B; no external load ^[2]	—	20	—	20	—	20	ns
		OE to A	—	200	—	200	—	200	ns
		OE to B	—	200	—	200	—	200	ns
t _{TLH}	LOW to HIGH output transition time	A port	2.8	7.4	2.6	6.6	1.8	6.2	ns
		B port	3.2	8.3	2.9	7.9	2.4	6.8	ns
t _{THL}	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.6	ns
t _{sk(o)}	output skew time	between channels ^[3]	—	0.7	—	0.7	—	0.7	ns
t _W	pulse width	data inputs	20	—	20	—	20	—	ns
f _{data}	data rate		—	50	—	50	—	50	Mbit/s
V _{CC(A)} = 3.3 V ± 0.3 V									
t _{PHL}	HIGH to LOW propagation delay	A to B	—	—	—	2.4	—	3.1	ns
t _{PLH}	LOW to HIGH propagation delay	A to B	—	—	—	4.2	—	4.4	ns
t _{PHL}	HIGH to LOW propagation delay	B to A	—	—	—	2.5	—	3.3	ns
t _{PLH}	LOW to HIGH propagation delay	B to A	—	—	—	2.5	—	2.6	ns
t _{en}	enable time	OE to A; B	—	—	—	200	—	200	ns
t _{dis}	disable time	OE to A; no external load ^[2]	—	—	—	15	—	15	ns
		OE to B; no external load ^[2]	—	—	—	15	—	15	ns
		OE to A	—	—	—	260	—	260	ns
		OE to B	—	—	—	200	—	200	ns
t _{TLH}	LOW to HIGH output transition time	A port	—	—	2.3	5.6	1.9	5.9	ns
		B port	—	—	2.5	6.4	2.1	7.4	ns

Dual supply translating transceiver; open-drain; auto direction sensing

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C^[1]...continuedVoltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t _{THL}	HIGH to LOW output transition time	A port	—	—	2.0	5.4	1.9	5.0	ns
		B port	—	—	2.3	7.4	2.4	7.6	ns
t _{sk(o)}	output skew time	between channels ^[3]	—	—	—	0.7	—	0.7	ns
t _W	pulse width	data inputs	—	—	20	—	20	—	ns
f _{data}	data rate		—	—	—	50	—	50	Mbit/s

[1] t_{en} is the same as t_{pZL} and t_{pZH}.t_{dis} is the same as t_{pLZ} and t_{pHZ}.

[2] Delay between OE going LOW and when the outputs are actually disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions	V _{CC(B)}							Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V			
			Min	Max	Min	Max	Min	Max		
V _{CC(A)} = 1.8 V ± 0.15 V										
t _{PHL}	HIGH to LOW propagation delay	A to B		—	5.8	—	5.9	—	7.3	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		—	8.5	—	8.5	—	8.8	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		—	5.5	—	5.7	—	5.9	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		—	6.7	—	5.7	—	0.7	ns
t _{en}	enable time	OE to A; B		—	200	—	200	—	200	ns
t _{dis}	disable time	OE to A; no external load	[2]	—	30	—	30	—	30	ns
		OE to B; no external load	[2]	—	30	—	30	—	30	ns
		OE to A		—	250	—	250	—	250	ns
		OE to B		—	220	—	220	—	220	ns
t _{TLH}	LOW to HIGH output transition time	A port		3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port		3.3	13.5	2.7	11.4	2.7	9.5	ns
t _{THL}	HIGH to LOW output transition time	A port		2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port		2.9	9.5	2.8	9.4	2.8	12.5	ns
t _{sk(o)}	output skew time	between channels	[3]	—	0.8	—	0.8	—	0.8	ns
t _W	pulse width	data inputs		20	—	20	—	20	—	ns

Dual supply translating transceiver; open-drain; auto direction sensing

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions		V _{CC(B)}						Unit
				2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	
f _{data}	data rate			—	50	—	50	—	50	Mbit/s
V _{CC(A)} = 2.5 V ± 0.2 V										
t _{PHL}	HIGH to LOW propagation delay	A to B		—	4.0	—	4.2	—	4.3	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		—	4.4	—	5.2	—	5.5	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		—	3.8	—	4.5	—	5.4	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		—	3.2	—	2.0	—	0.9	ns
t _{en}	enable time	OE to A; B		—	200	—	200	—	200	ns
t _{dis}	disable time	OE to A; no external load	[2]	—	25	—	25	—	25	ns
		OE to B; no external load	[2]	—	25	—	25	—	25	ns
		OE to A		—	220	—	220	—	220	ns
		OE to B		—	220	—	220	—	220	ns
t _{TLH}	LOW to HIGH output transition time	A port		2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port		3.2	10.4	2.9	9.7	2.4	8.3	ns
t _{THL}	HIGH to LOW output transition time	A port		1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port		2.2	9.8	2.4	8.4	2.6	8.3	ns
t _{sk(o)}	output skew time	between channels	[3]	—	0.8	—	0.8	—	0.8	ns
t _W	pulse width	data inputs		20	—	20	—	20	—	ns
f _{data}	data rate			—	50	—	50	—	50	Mbit/s
V _{CC(A)} = 3.3 V ± 0.3 V										
t _{PHL}	HIGH to LOW propagation delay	A to B		—	—	—	3.0	—	3.9	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		—	—	—	5.3	—	5.5	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		—	—	—	3.2	—	4.2	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		—	—	—	3.2	—	3.3	ns
t _{en}	enable time	OE to A; B		—	—	—	200	—	200	ns
t _{dis}	disable time	OE to A; no external load	[2]	—	—	—	20	—	20	ns
		OE to B; no external load	[2]	—	—	—	20	—	20	ns

Dual supply translating transceiver; open-drain; auto direction sensing

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 9](#); for wave forms see [Figure 7](#) and [Figure 8](#).

Symbol	Parameter	Conditions		V _{CC(B)}						Unit
				2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	
		OE to A		—	—	—	280	—	280	ns
		OE to B		—	—	—	220	—	220	ns
t _{TLH}	LOW to HIGH output transition time	A port		—	—	2.3	7.0	1.9	7.4	ns
		B port		—	—	2.5	8.0	2.1	9.3	ns
t _{THL}	HIGH to LOW output transition time	A port		—	—	2.0	6.8	1.9	6.3	ns
		B port		—	—	2.3	9.3	2.4	9.5	ns
t _{sk(o)}	output skew time	between channels	[3]	—	—	—	0.8	—	0.8	ns
t _W	pulse width	data inputs		—	—	20	—	20	—	ns
f _{data}	data rate			—	—	—	50	—	50	Mbit/s

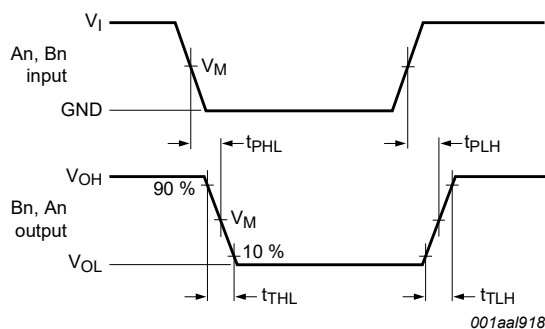
[1] t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[2] Delay between OE going LOW and when the outputs are actually disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

12 Waveforms



Measurement points are given in [Table 12](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. The data input (An, Bn) to data output (Bn, An) propagation delay times

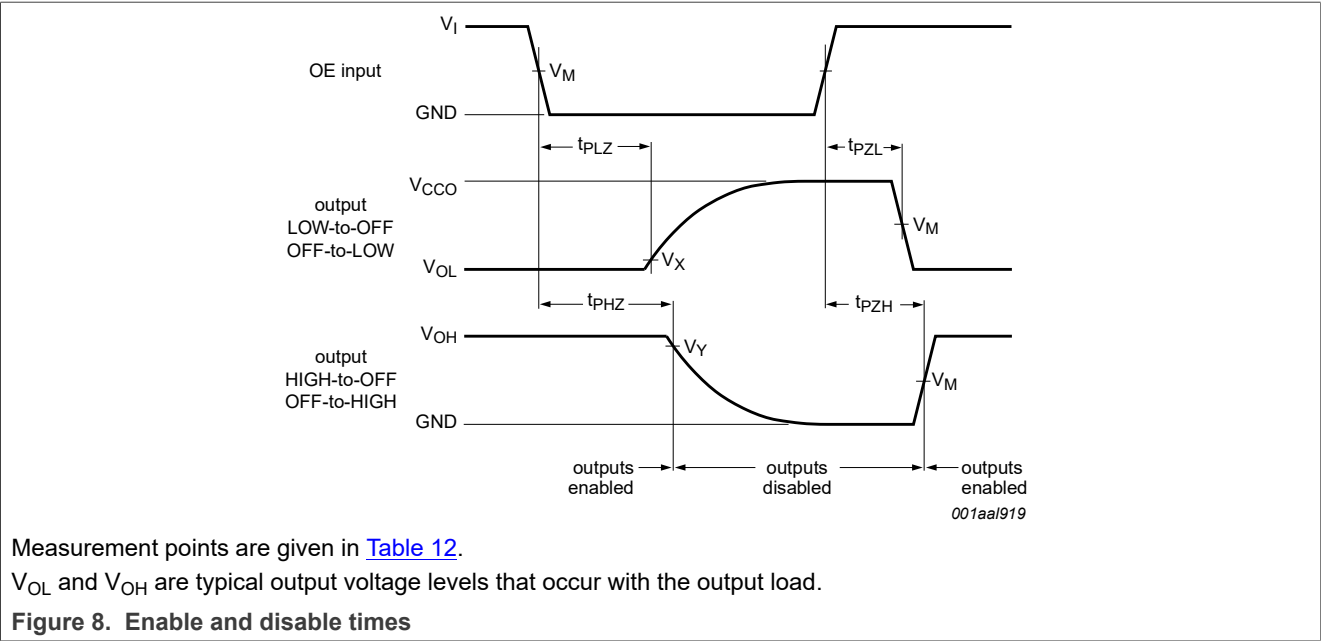
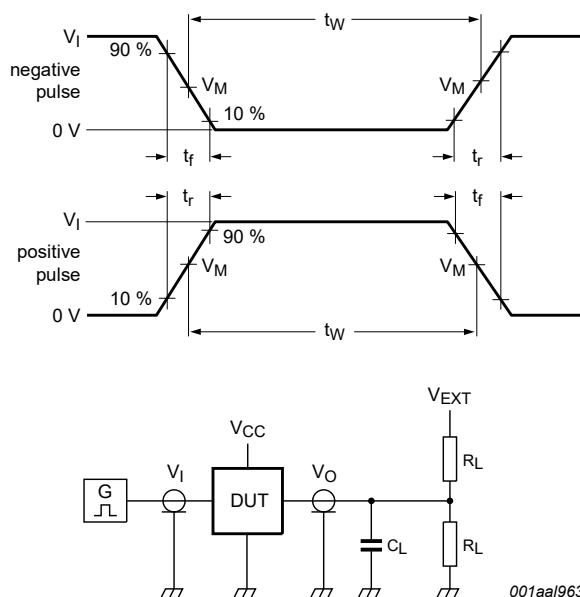


Table 12. Measurement points^{[1][2]}

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.

Dual supply translating transceiver; open-drain; auto direction sensing



Test data is given in Table 13.

All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$; $Z_O = 50 \text{ }\Omega$; $dV/dt \geq 1.0 \text{ V/ns}$.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Figure 9. Test circuit for measuring switching times

Table 13. Test data

Supply voltage		Input		Load		V _{EXT}		
V _{CC(A)}	V _{CC(B)}	V _I ^[1]	Δt/ΔV	C _L	R _L ^[2]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ} ^[3]
1.65 V to 3.6 V	2.3 V to 5.5 V	V _{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V _{CCO}

[1] V_{CC1} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay, and output rise and fall measurements, $R_L = 1\text{ M}\Omega$; for measuring enable and disable times, $R_L = 50\text{ K}\Omega$.

[3] V_{CCQ} is the supply voltage associated with the output.

13 Application information

13.1 Applications

Voltage level-translation applications. The NTS0102 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I²C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports, however the NTB0102 may be more suitable.

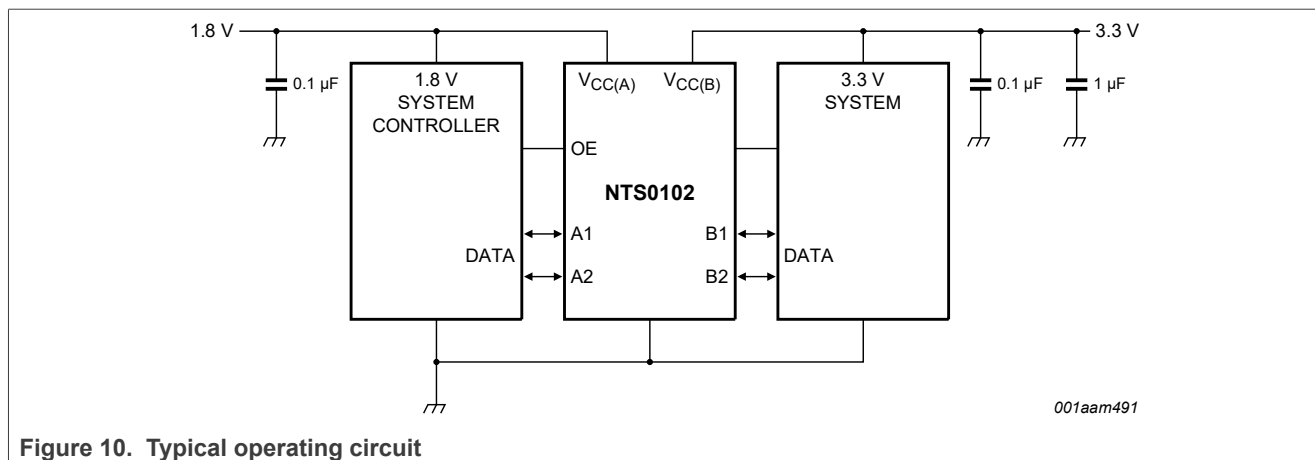


Figure 10. Typical operating circuit

13.2 Architecture

The architecture of the NTS0102 is shown in [Figure 11](#). The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

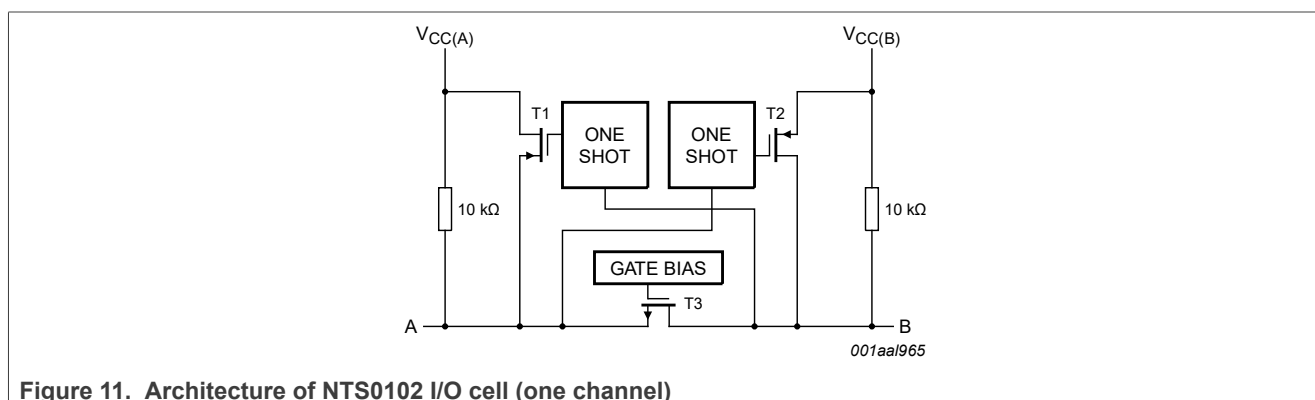


Figure 11. Architecture of NTS0102 I/O cell (one channel)

The NTS0102 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 kΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CC}/2$; it is de-activated approximately 50 ns after the output reaches $V_{CC}/2$. During the acceleration time, the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic I_{CC} , the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

13.3 Input driver requirements

As the NTS0102 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}), and propagation delay (t_{PHL}) are

dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50 Ω is used.

13.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output will not reach the positive rail within the one-shot pulse duration.

To avoid excessive capacitive loading, and to ensure correct triggering of the one-shot, it's recommended to use short trace lengths and low capacitance connectors on NTS0102 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns).

13.5 Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0102 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

13.6 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW

causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

13.7 Pull-up or pull-down resistors on I/Os lines

Each A port I/O has an internal 10 k Ω pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 k Ω pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 k Ω , this effects the V_{OL} level. When OE goes LOW the internal pull-ups of the NTS0102 are disabled.

13.8 GD package vs TL package

Due to differences in package construction the TL package has a center pad vs no center pad for the GD package. The following section provides guidance in replacement vs new applications.

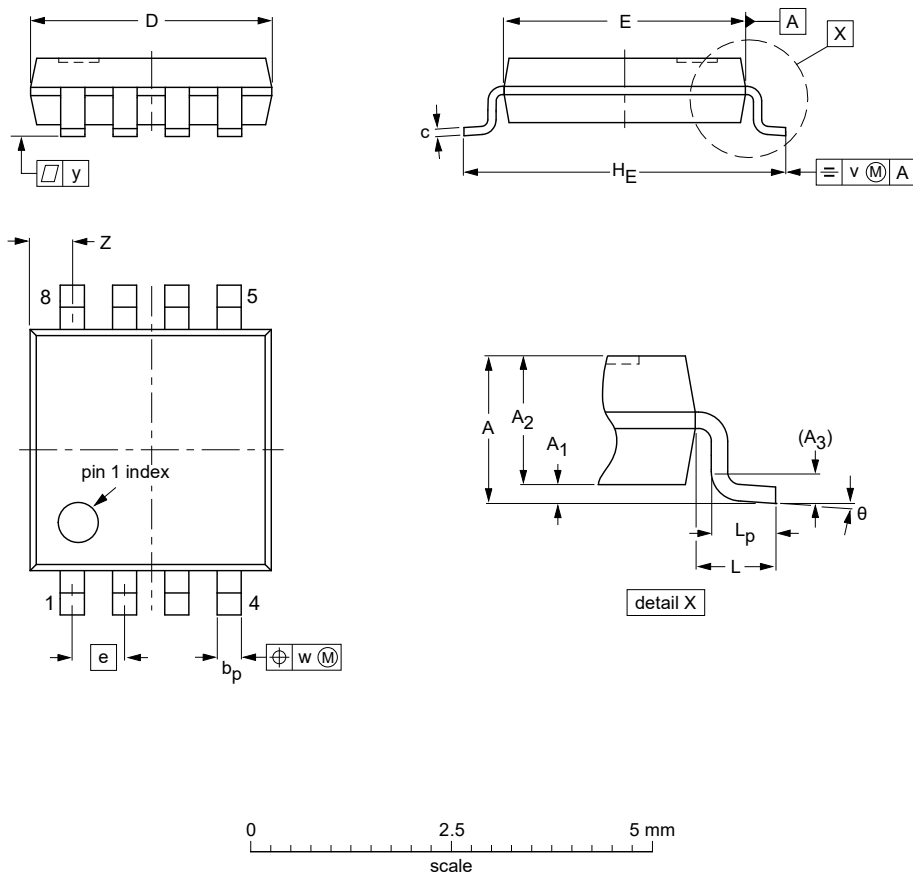
- **No trace under GD package**

1. Replacement of GD package: The pad is not electrically connected to the silicon (no wire bond and epoxy is not conductive) and can be left floating. It is not required to be connected to the PCB. Simply place the TL package on the same PCB traces as the existing GD package.

2. New use of the TL package: Place PCB trace for soldering of the center pad based on PCB layout recommendations for better mechanical connection and thermal conductivity. The PCB center pad can be connect to GND or left floating.
- **Trace under the GD package**
 1. Replacement of GD package: It is not best practice to have center pad over the trace but since the TL package center pad is not connected to the silicon the risk is low. If there are multiple traces there could be EMI and cross talk. In both cases the customer needs to evaluate risk.
 2. New use of the TL package: Do not route traces under the package

14 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

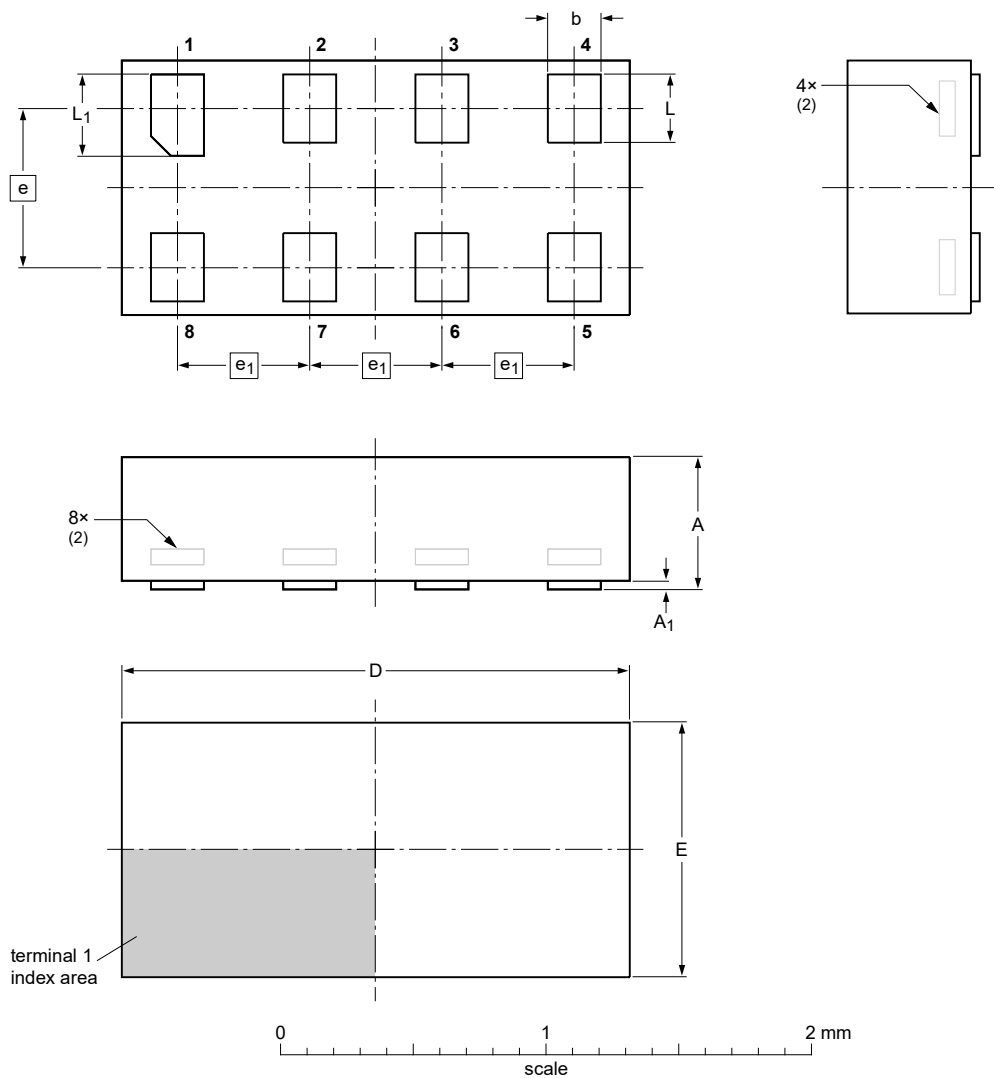
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Figure 12. Package outline SOT505-2 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

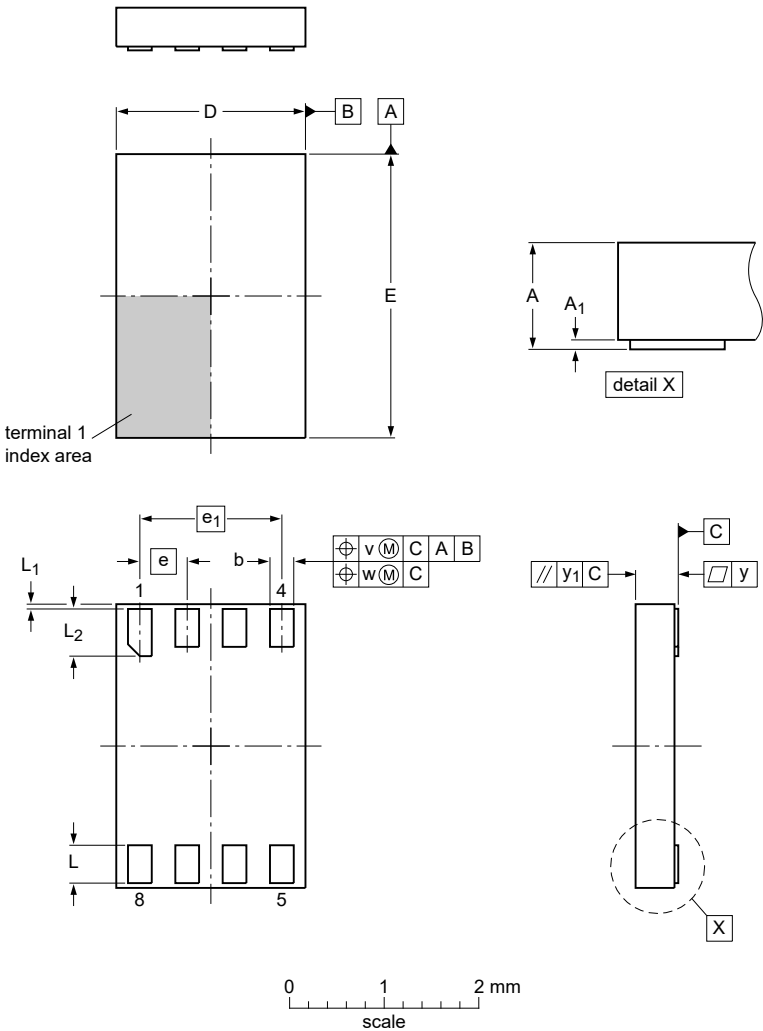
- Notes
- 1. Including plating thickness.
 - 2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	---	MO-252	---			07-11-14 07-12-07

Figure 13. Package outline SOT833-1 (XSON8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	b	D	E	e	e ₁	L	L ₁	L ₂	v	w	y	y ₁
max		0.05	0.35	2.1	3.1			0.5	0.15	0.6				
nom	0.5					0.5	1.5				0.1	0.05	0.05	0.1
min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						07-12-21 12-11-20

Figure 14. Package outline SOT996-2 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

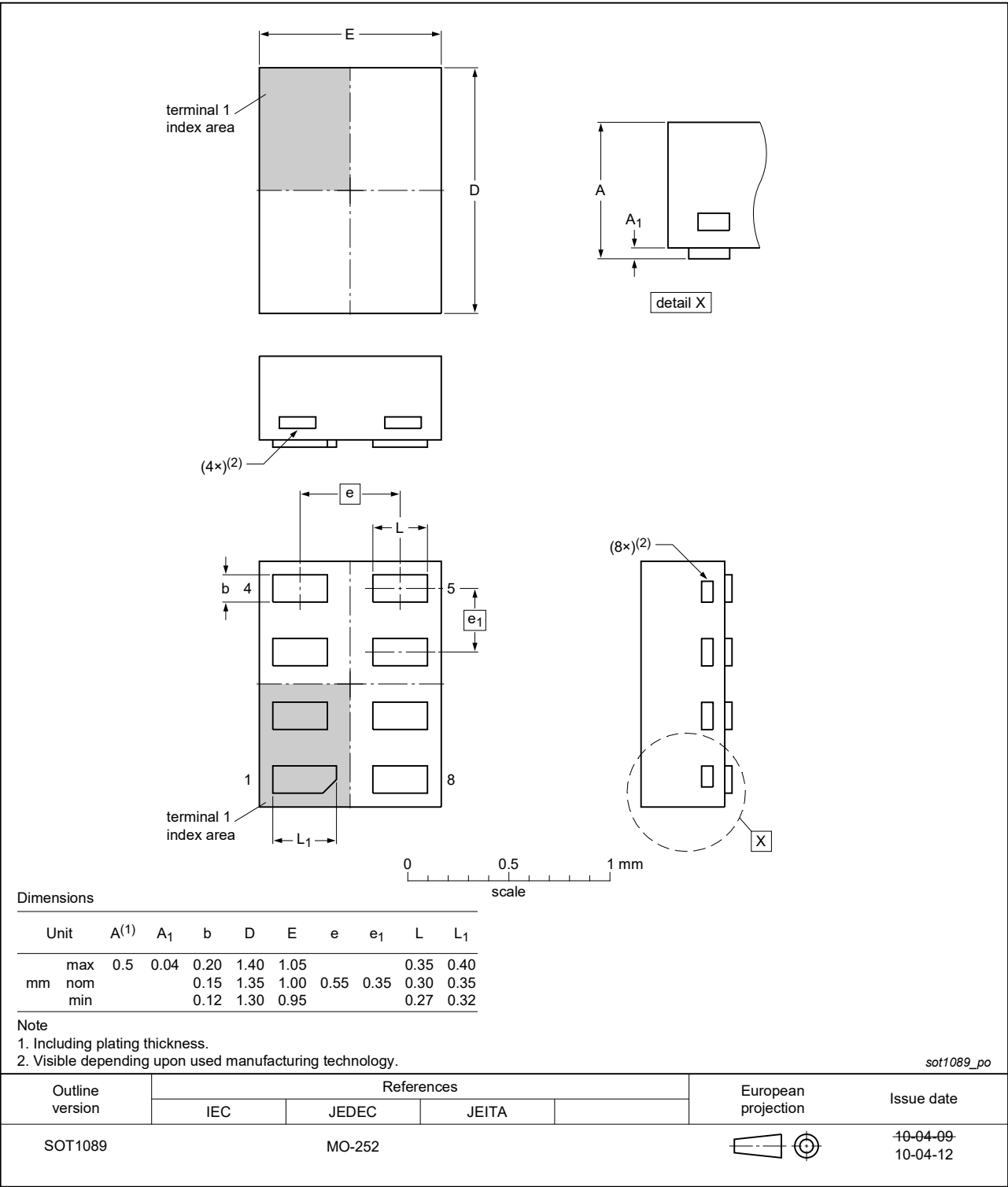
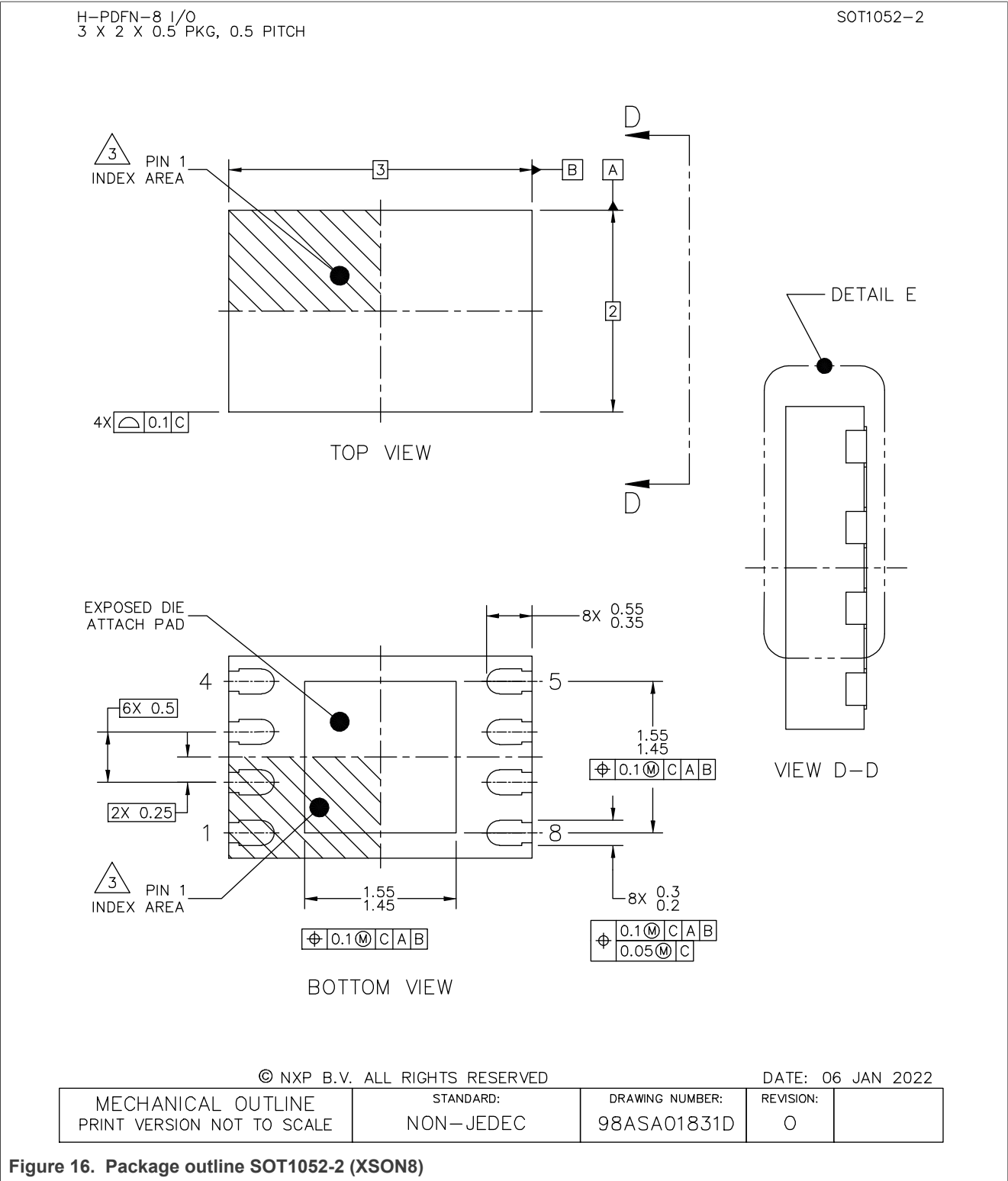
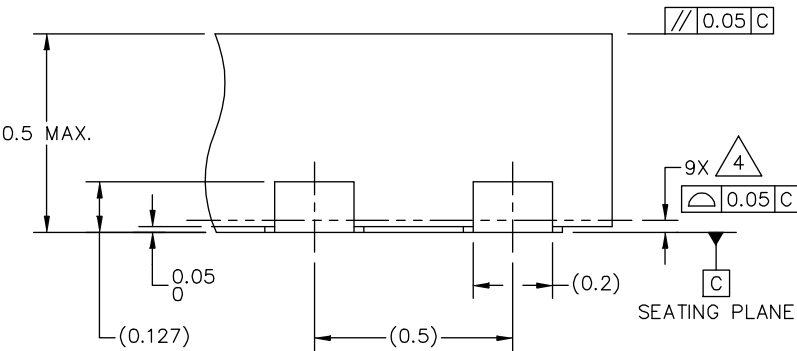


Figure 15. Package outline SOT1089 (XSON8)



H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



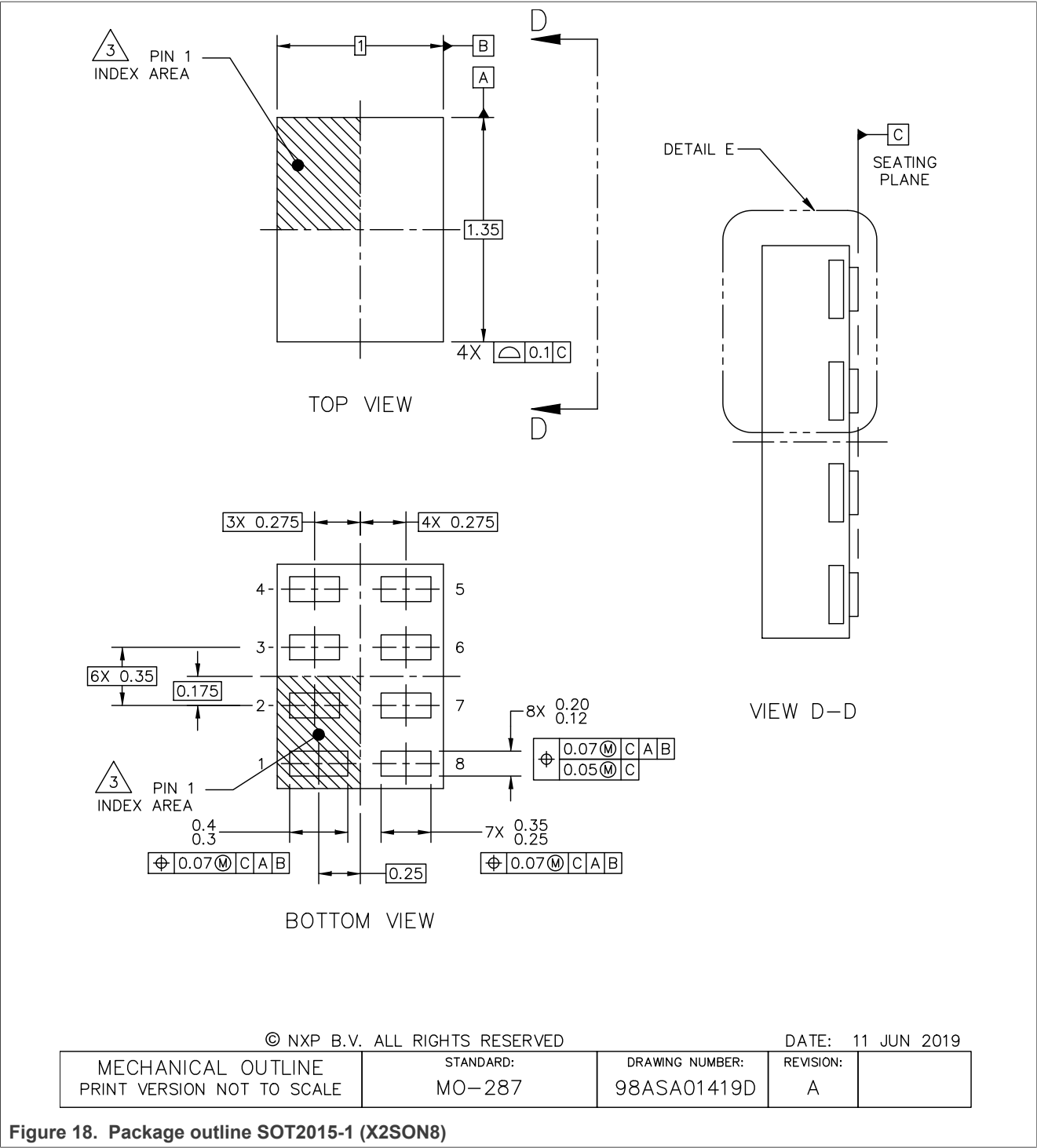
DETAIL E
VIEW ROTATED 90° CW

© NXP B.V. ALL RIGHTS RESERVED

DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: O	
--	------------------------	--------------------------------	----------------	--

Figure 17. Package outline SOT1052-2 (XSON8)



15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “*Surface mount reflow soldering description*”.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [Table 15](#)

Table 14. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.
Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).

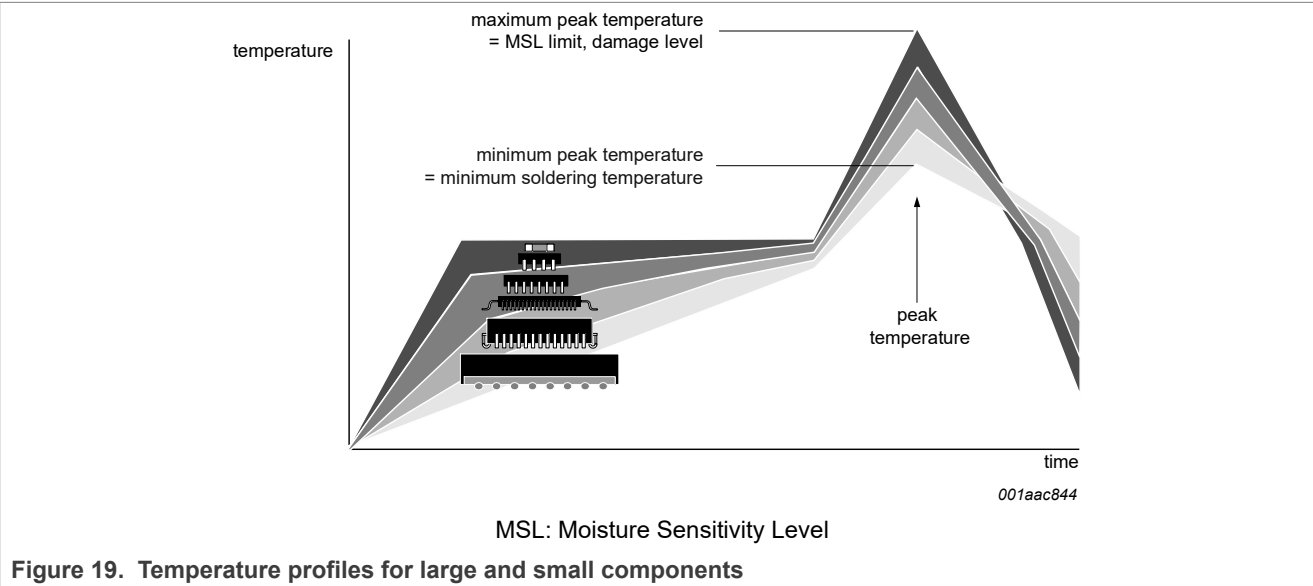


Figure 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

16 Soldering: PCB footprints

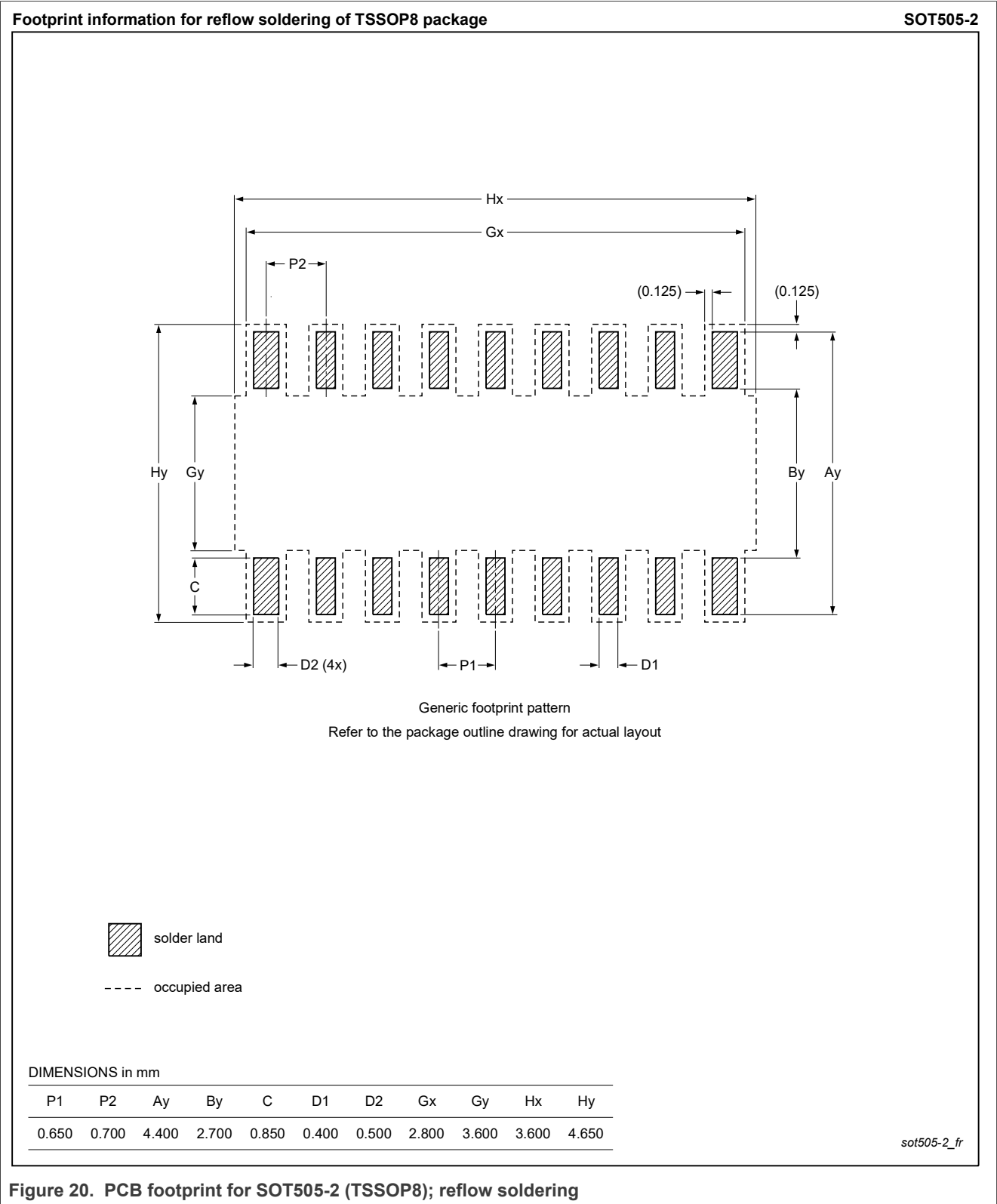
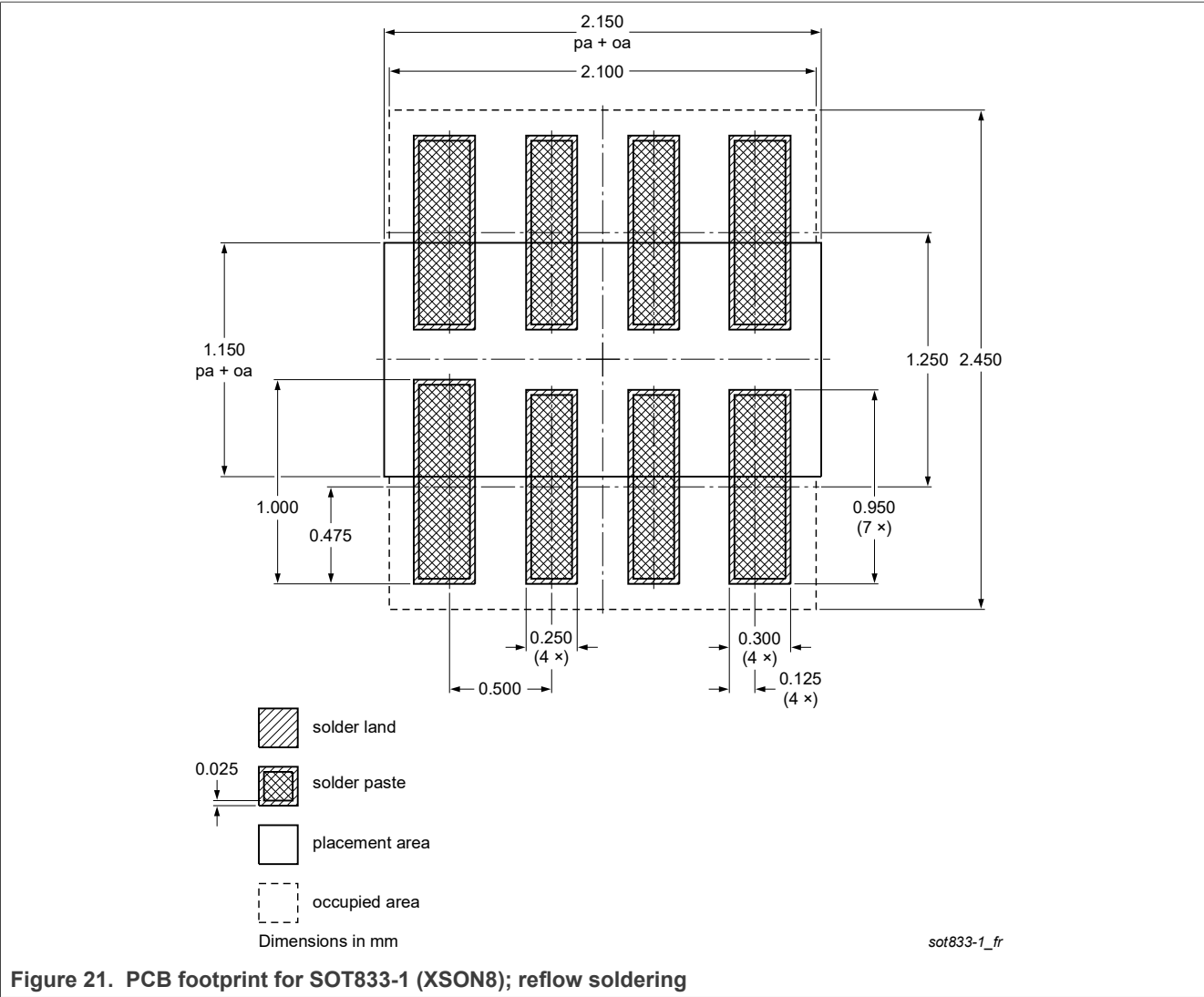


Figure 20. PCB footprint for SOT505-2 (TSSOP8); reflow soldering



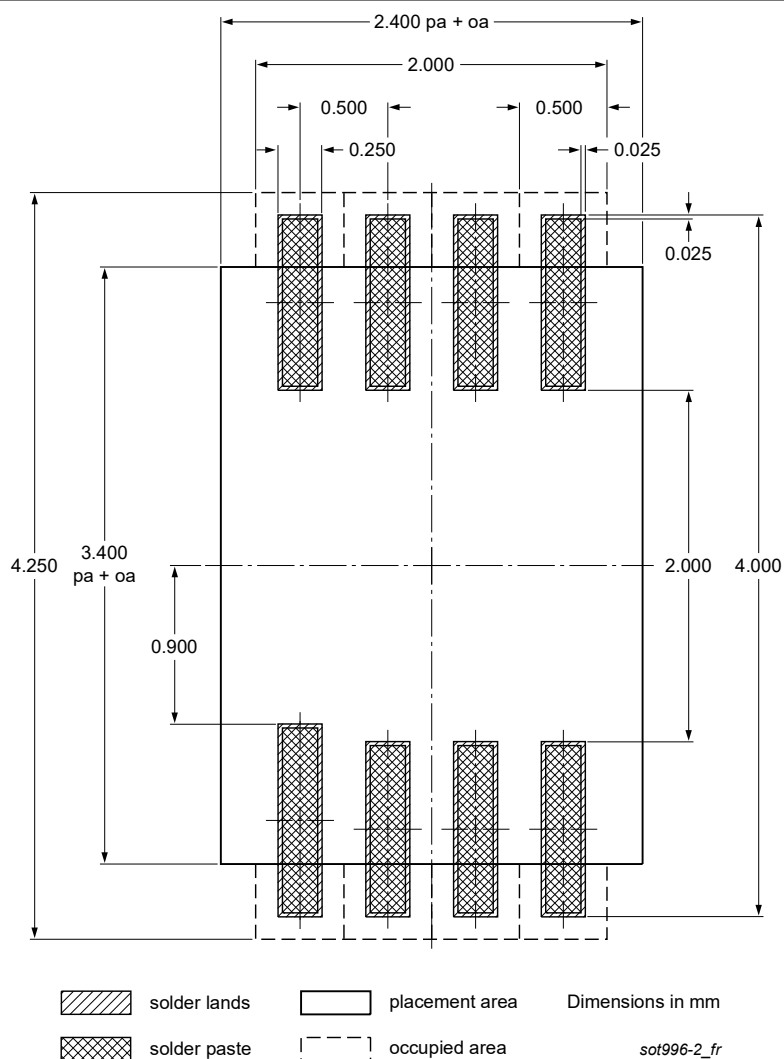
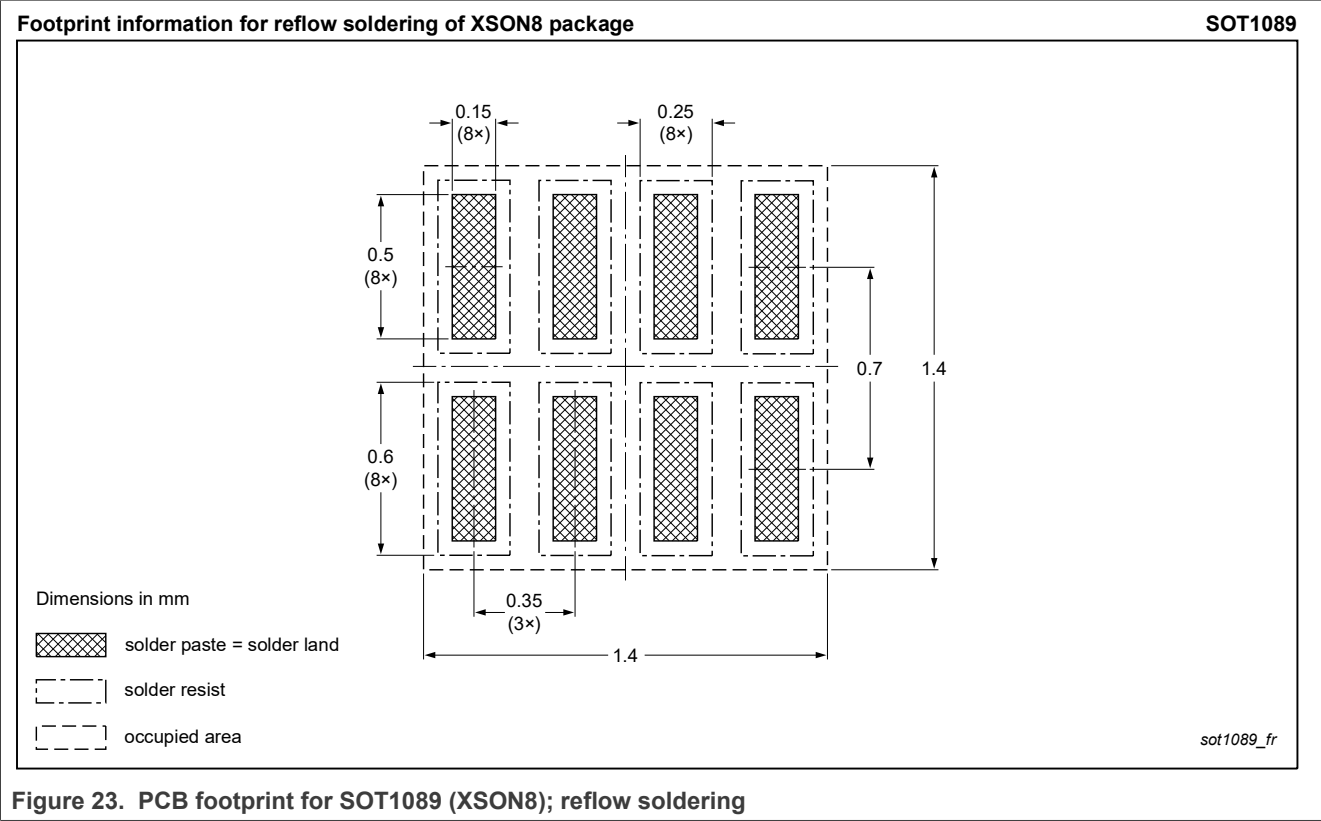
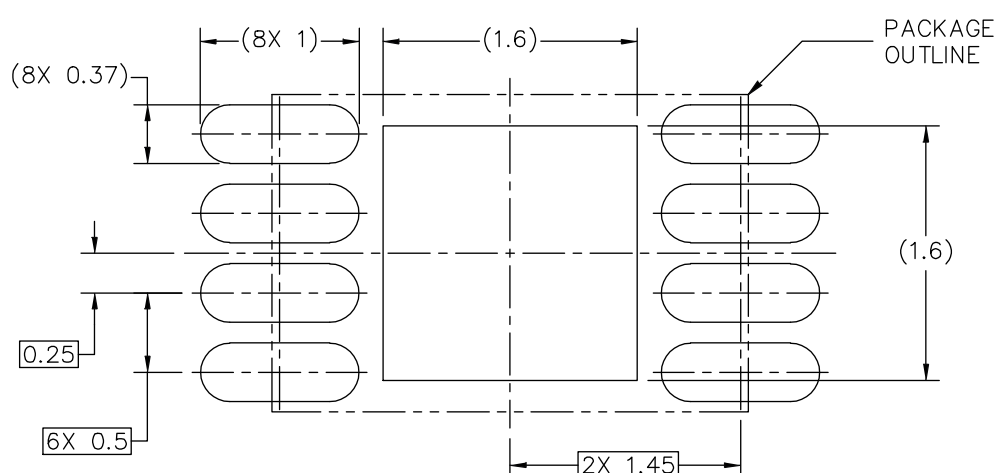


Figure 22. PCB footprint for SOT996-2 (XSON8U); reflow soldering



H-PDFN-8 1/0
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



PCB DESIGN GUIDELINES

RECOMMENDED SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

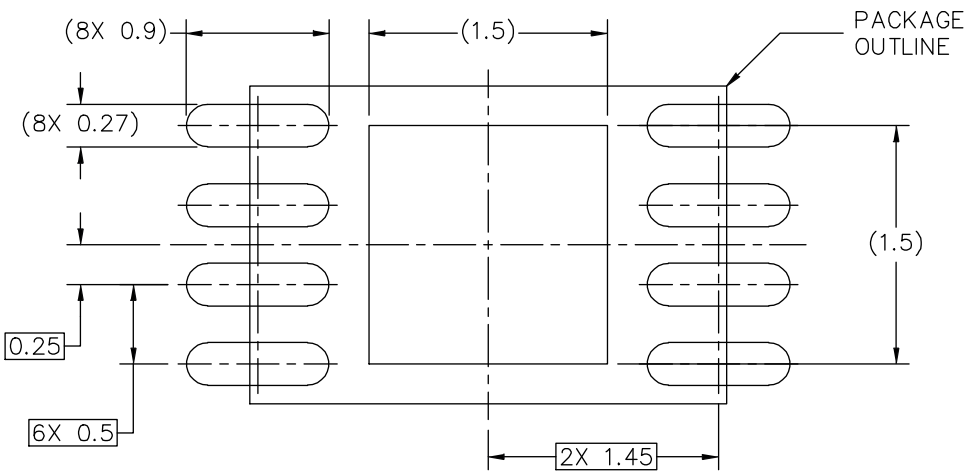
DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: 0
--	------------------------	--------------------------------	----------------

Figure 24. PCB footprint for SOT1052-2 (XSON8); recommended solder mask opening pattern

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



PCB DESIGN GUIDELINES
RECOMMENDED I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

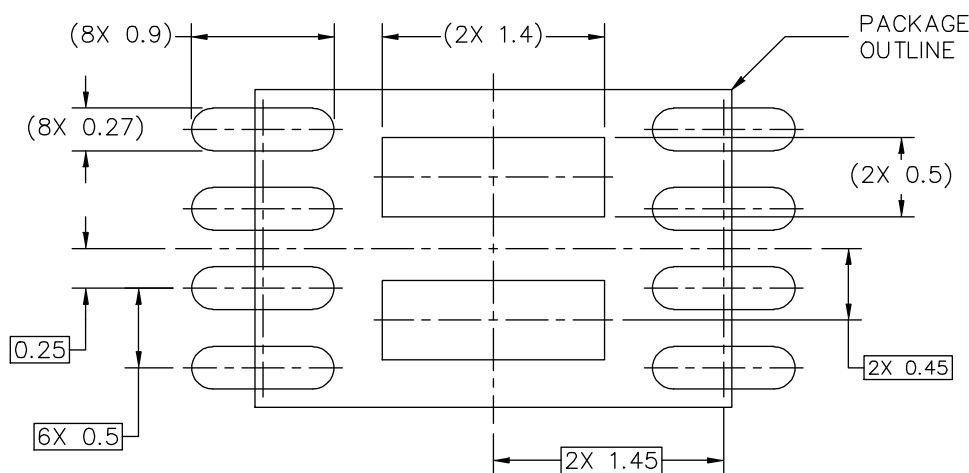
DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: O	
--	------------------------	--------------------------------	----------------	--

Figure 25. PCB footprint for SOT1052-2 (XSON8); recommended I/O pads and solderable area

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – RECOMMENDED SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: O	
--	------------------------	--------------------------------	----------------	--

Figure 26. PCB footprint for SOT1052-2 (XSON8); recommended solder paste stencil

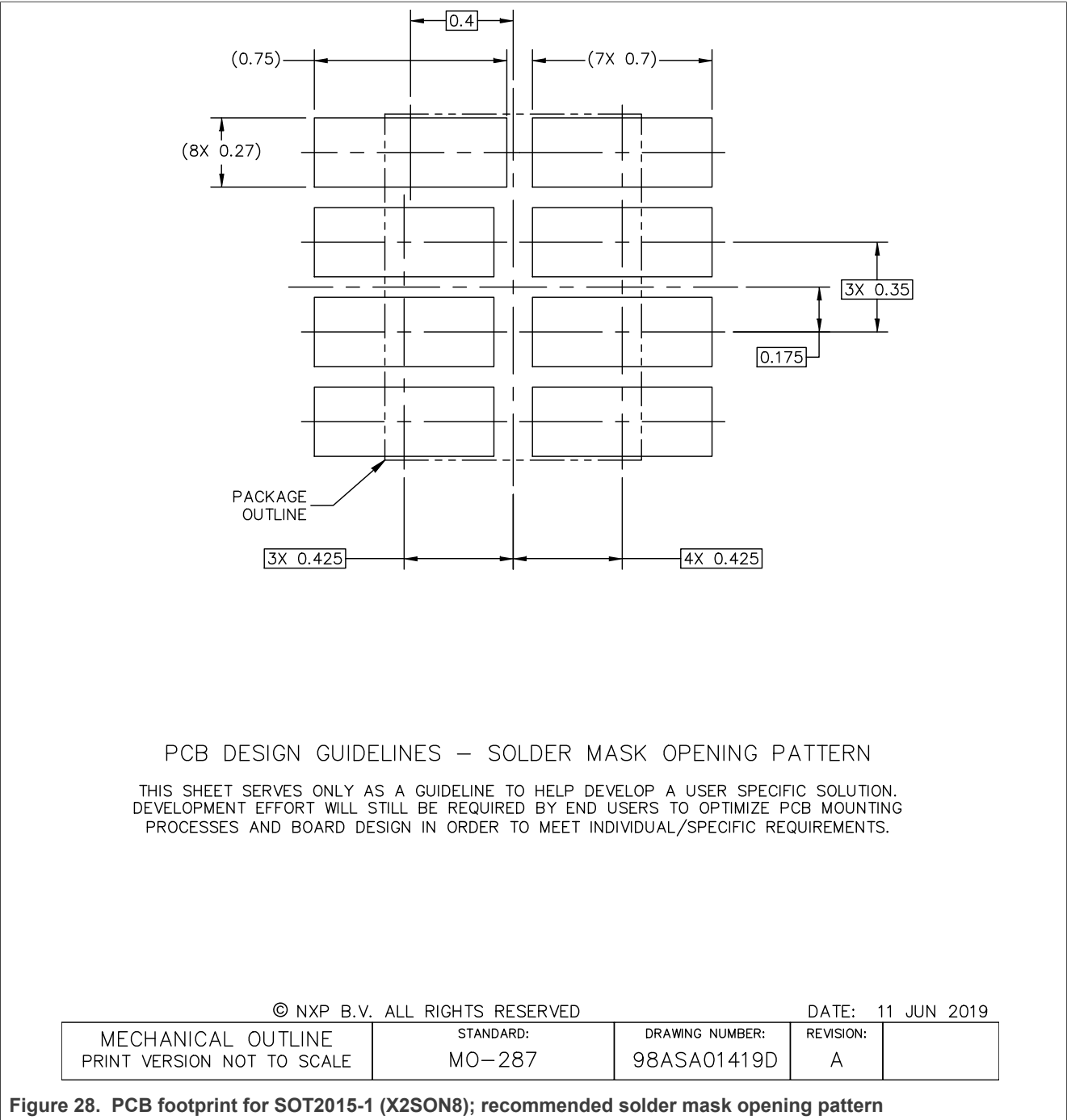
H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

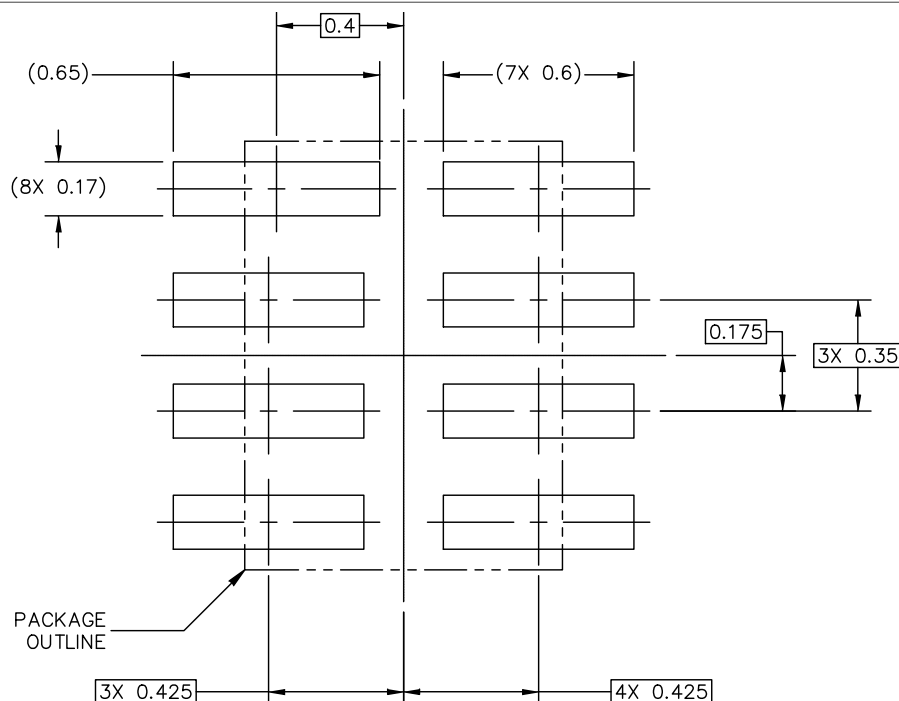
SOT1052-2

- NOTES:
- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 - 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - 3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
 - 4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
 - 5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

© NXP B.V. ALL RIGHTS RESERVED		DATE: 06 JAN 2022		
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: 0	

Figure 27. PCB footprint for SOT1052-2 (XSON8); notes



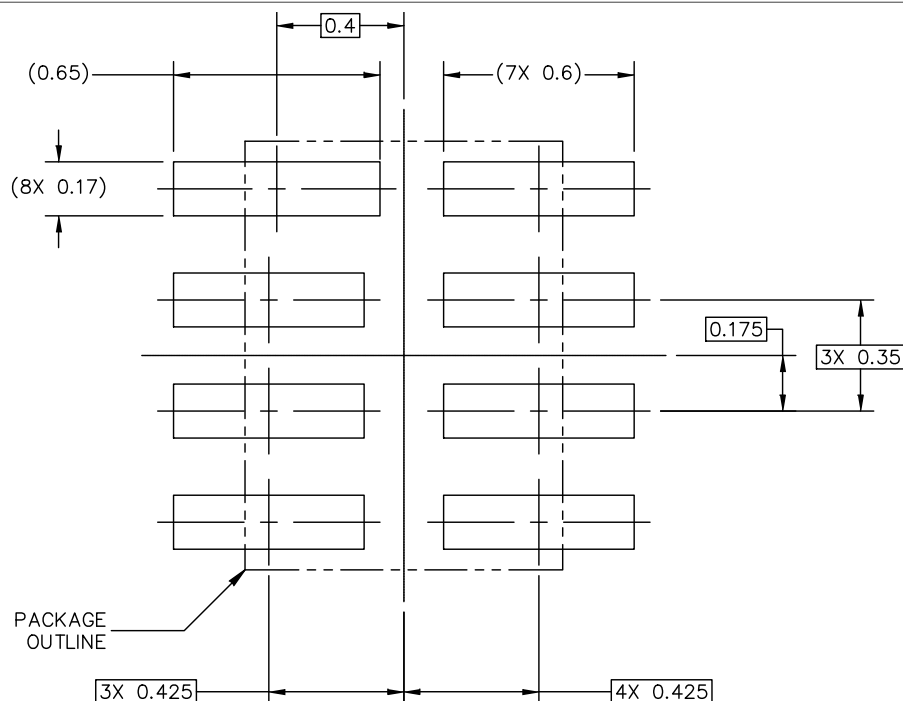


PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED			DATE: 11 JUN 2019	
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-287	DRAWING NUMBER: 98ASA01419D	REVISION: A	

Figure 29. PCB footprint for SOT2015-1 (X2SON8); recommended I/O pads and solderable area



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 11 JUN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-287	DRAWING NUMBER: 98ASA01419D	REVISION: A
--	---------------------	--------------------------------	----------------

Figure 30. PCB footprint for SOT2015-1 (X2SON8); recommended solder paste stencil

- NOTES:
- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 - 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - 3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
 - 4. COPLANARITY APPLIES TO LEADS.
 - 5. MIN METAL GAP SHOULD BE 0.15 MM.

© NXP B.V. ALL RIGHTS RESERVED		DATE: 11 JUN 2019		
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-287	DRAWING NUMBER: 98ASA01419D	REVISION: A	

Figure 31. PCB footprint for SOT2015-1 (X2SON8); notes

17 Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I ² C	Inter-Integrated Circuit
MM	Machine Model
PCB	Printed-circuit board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter
UTLP	Ultra Thin Leadless Package

18 Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0102 v.4.5	20230706	Product data sheet	—	NTS0102 v.4.4
Modifications:	• Added type number NTS0102JK			
NTS0102 v.4.4	20221006	Product data sheet	202210008I	NTS0102 v.4.3
NTS0102 v.4.3	20220420	Product data sheet	—	NTS0102 v.4.2
NTS0102 v.4.2	20220303	Product data sheet	—	NTS0102 v.4.1
NTS0102 v.4.1	20211112	Product data sheet	—	NTS0102 v.4
NTS0102 v.4	20130123	Product data sheet	—	NTS0102 v.3
NTS0102 v.3	20111117	Product data sheet	—	NTS0102 v.2
NTS0102 v.2	20110411	Product data sheet	—	NTS0102 v.1
NTS0102 v.1	20100921	Product data sheet	—	—

19 Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

19.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Dual supply translating transceiver; open-drain; auto direction sensing

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

19.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Ordering information	1	Tab. 10.	Dynamic characteristics for temperature range -40 °C to +85 °C	8
Tab. 2.	Ordering options	2	Tab. 11.	Dynamic characteristics for temperature range -40 °C to +125 °C	10
Tab. 3.	Pin description	4	Tab. 12.	Measurement points	13
Tab. 4.	Function table	4	Tab. 13.	Test data	14
Tab. 5.	Limiting values	5	Tab. 14.	SnPb eutectic process (from J-STD-020D)	26
Tab. 6.	Recommended operating conditions	5	Tab. 15.	Lead-free process (from J-STD-020D)	26
Tab. 7.	Typical static characteristics	6	Tab. 16.	Abbreviations	39
Tab. 8.	Typical supply current	6	Tab. 17.	Revision history	39
Tab. 9.	Static characteristics	6			

Figures

Fig. 1.	Logic symbol	3	Fig. 21.	PCB footprint for SOT833-1 (XSON8); reflow soldering	28
Fig. 2.	Pin configuration SOT505-2 (TSSOP8)	3	Fig. 22.	PCB footprint for SOT996-2 (XSON8U); reflow soldering	29
Fig. 3.	Pin configuration SOT833-1 (XSON8) and SOT1089 (XSON8)	3	Fig. 23.	PCB footprint for SOT1089 (XSON8); reflow soldering	30
Fig. 4.	Pin configuration SOT996-2 (XSON8)	4	Fig. 24.	PCB footprint for SOT1052-2 (XSON8); recommended solder mask opening pattern ...	31
Fig. 5.	Pin configuration SOT1052-2 (XSON8)	4	Fig. 25.	PCB footprint for SOT1052-2 (XSON8); recommended I/O pads and solderable area	32
Fig. 6.	Pin configuration SOT2015-1 (X2SON8)	4	Fig. 26.	PCB footprint for SOT1052-2 (XSON8); recommended solder paste stencil	33
Fig. 7.	The data input (An, Bn) to data output (Bn, An) propagation delay times	12	Fig. 27.	PCB footprint for SOT1052-2 (XSON8); notes	34
Fig. 8.	Enable and disable times	13	Fig. 28.	PCB footprint for SOT2015-1 (X2SON8); recommended solder mask opening pattern ...	35
Fig. 9.	Test circuit for measuring switching times	14	Fig. 29.	PCB footprint for SOT2015-1 (X2SON8); recommended I/O pads and solderable area	36
Fig. 10.	Typical operating circuit	15	Fig. 30.	PCB footprint for SOT2015-1 (X2SON8); recommended solder paste stencil	37
Fig. 11.	Architecture of NTS0102 I/O cell (one channel)	15	Fig. 31.	PCB footprint for SOT2015-1 (X2SON8); notes	38
Fig. 12.	Package outline SOT505-2 (TSSOP8)	18			
Fig. 13.	Package outline SOT833-1 (XSON8)	19			
Fig. 14.	Package outline SOT996-2 (XSON8)	20			
Fig. 15.	Package outline SOT1089 (XSON8)	21			
Fig. 16.	Package outline SOT1052-2 (XSON8)	22			
Fig. 17.	Package outline SOT1052-2 (XSON8)	23			
Fig. 18.	Package outline SOT2015-1 (X2SON8)	24			
Fig. 19.	Temperature profiles for large and small components	26			
Fig. 20.	PCB footprint for SOT505-2 (TSSOP8); reflow soldering	27			

Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	1
4.1	Ordering options	2
5	Functional diagram	3
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	4
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
11	Dynamic characteristics	8
12	Waveforms	12
13	Application information	14
13.1	Applications	14
13.2	Architecture	15
13.3	Input driver requirements	15
13.4	Output load considerations	16
13.5	Power up	16
13.6	Enable and disable	16
13.7	Pull-up or pull-down resistors on I/Os lines	16
13.8	GD package vs TL package	16
14	Package outline	18
15	Soldering of SMD packages	25
15.1	Introduction to soldering	25
15.2	Wave and reflow soldering	25
15.3	Wave soldering	25
15.4	Reflow soldering	25
16	Soldering: PCB footprints	27
17	Abbreviations	39
18	Revision history	39
19	Legal information	40

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.