Mask Set Errata for Mask 2N36S

This report applies to mask 2N36S for these products:

- MKE1xZ256VLL7
- MKE1xZ256VLH7
- MKE1xZ128VLL7
- MKE1xZ128VLH7

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR050117	FAC: Execute-only access control feature has been deprecated
ERR009380	FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang
ERR010364	LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer
ERR050181	LPIT CVAL cannot be read correctly during timer running
ERR010527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
ERR010355	PWT : Read/write resevered address (40056008~40056fff) won't result in hard fault interrupt
ERR010536	WDOG: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before the next block

Table 2. Revision History

Revision	Changes
06Apr2021	Initial revision

ERR050117: FAC: Execute-only access control feature has been deprecated

Description: The FAC feature is no longer recommended for use.

Workaround: Do not program the XACCn registers to use the FAC feature.

ERR009380: FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang

Description: Accessing a FlexIO register when the FlexIO functional clock is disabled (the clock source configured to 0 in PCC_FLEXIO0[PCS], or the selected clock source is disabled) will hang the bus and the access will stall forever.

Workaround: Always enable the FlexIO functional clock before accessing any FlexIO register.

ERR010364: LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer

Description: If the transmit FIFO is empty at the end of a master receive transfer and the AUTOSTOP (MCFGR1[AUTOSTOP]) bit in the Master Configuration Register 1 is clear, the LPI2C master sends a STOP condition before the next repeated START condition.

Workaround: Use software or DMA to queue up the subsequent transfer in the transmit FIFO before the completion of the master-receive transfer.

ERR050181: LPIT CVAL cannot be read correctly during timer running

Description: Customer reported a LPIT CVAL reading issue, that CVAL cannot be read correctly during timer running.

The root cause per IP owner feedback is:

The LPIT implements a functional clock domain for the counter and a bus clock domain for the register interface. The CVAL register increments on each clock cycle, but reading the register value is not synchronized when it changes clock domains. This can result in the CVAL register not being read correctly (eg: read returns some bits from previous cycle and some bits from next cycle).

Workaround: While the timer is running, CVALn register reads may not return the real value. If the timer value needs to be read,

read it during an LPIT interrupt service routine.

ERR010527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description: When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround: To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

ERR010355: PWT : Read/write resevered address (40056008~40056fff) won’t result in hard fault interrupt

Description: PWT : Read/write resevered address (40056008~40056fff) won’t result in hard fault interrupt

Workaround: Not writting to resevered address (40056008~40056fff).

ERR010536: WDOG: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before the next block

Description: WDOG cannot be unlocked if the unlock magic word are executed immediately after the RCS assert.

Workaround: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before next block.

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