Freescale Semiconductor
Chip Errata

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MC13201

2.4 GHz Low Power Transceiver for 802.15.4

1 Introduction

These errata pertains to all MC13201 production devices. The related IC Data Sheet, MC13201, and Reference Manual, MC13201RM apply to these devices. This document is included in shipments for which this errata applies.

2 IEEE 802.15.4 Transceiver Errata

The transceiver on the MC13201 is a separate die. The errata described in Table 1 applies.

Table 1. MC13201 Transceiver Errata

No	Errata	Work Around
1	The Doze current (no CLKO output active) is specified as 35 µA (typical) on the data sheet with the programmed CLKO frequency at a default of 32.786 kHz. This Doze current can be considerably higher for certain combinations of higher CLKO frequencies and event timer prescale options. These combinations consist of: a) CLKO freq = 16 MHZ with prescale select at 5, 6, or 7. b) CLKO freq = 8 MHZ with prescale select at 6, or 7. c) CLKO freq = 4 MHZ with prescale select at 7. All other combinations have no problems. The higher current will not occur every time Doze is enabled. There is no potential harm either to the transceiver or its operation. The Doze current is simply higher.	To work around this issue, there are three choices: a) Accept higher current in Doze mode. b) Do not use any of the described combinations in Doze mode. c) If a higher CLKO frequency is desired when using CLKO as an MCU clock source, and the desired prescale select can cause a problem, just before entering Doze mode, program the CLKO frequency to a lower value. Next, use the desired prescale value while in Doze. Finally, after exiting Doze mode, reprogram CLKO to the desired frequency before releasing the MCU clock to the CLKO source.
2	Timer Comparator 3 can abort an RX sequence - If an RX sequence (Packet Mode or Streaming Mode) is active and Timer Comp 3 matches the value of the Event Timer “current time” counter, the RX sequence will be aborted. No status bit is set and no interrupt can be generated. Exit from RX mode can only be detected by using GPIO1 as an “out-of-idle” indicator. Freescale’s IEEE 802.15.4 MAC and by inference all associated network stacks compensate for this situation. If users are writing their own software (such as using SMAC), this condition should be compensated for.	For users writing their own application: a) Never let the counter reach the compare value in Time Comp 3 register. b) Enable Timer Compare 3 always to generate an interrupt. If the interrupt occurs and the RX state was enabled. Take appropriate action, such as restarting RX. c) Monitor the “out-of_idle” indicator while in RX mode.
3	For proper performance of the radio the following modem registers must be over-programmed as shown below: • Write Register 0x31 to 0xA0C0 • Write Register 0x34 to 0xFEC6 Software can confirm the transceiver version that requires the register over-writes by reading the modem SPI Chip-ID Register, Address 0x2C. Register 0x2C reads as 0x6800 for this device.	• Write Register 0x31 to 0xA0C0 • Write Register 0x34 to 0xFEC6

NOTES

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