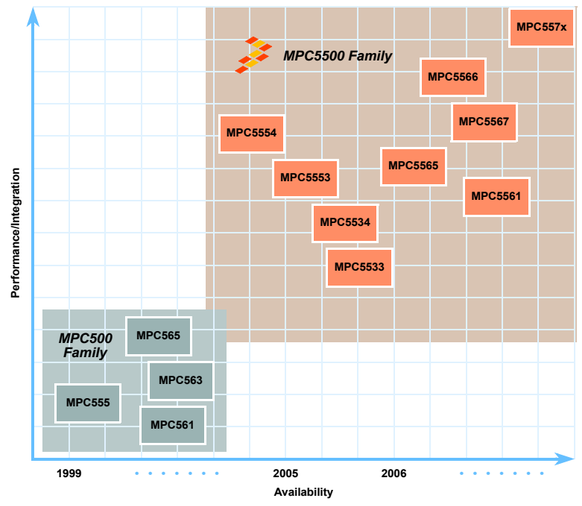
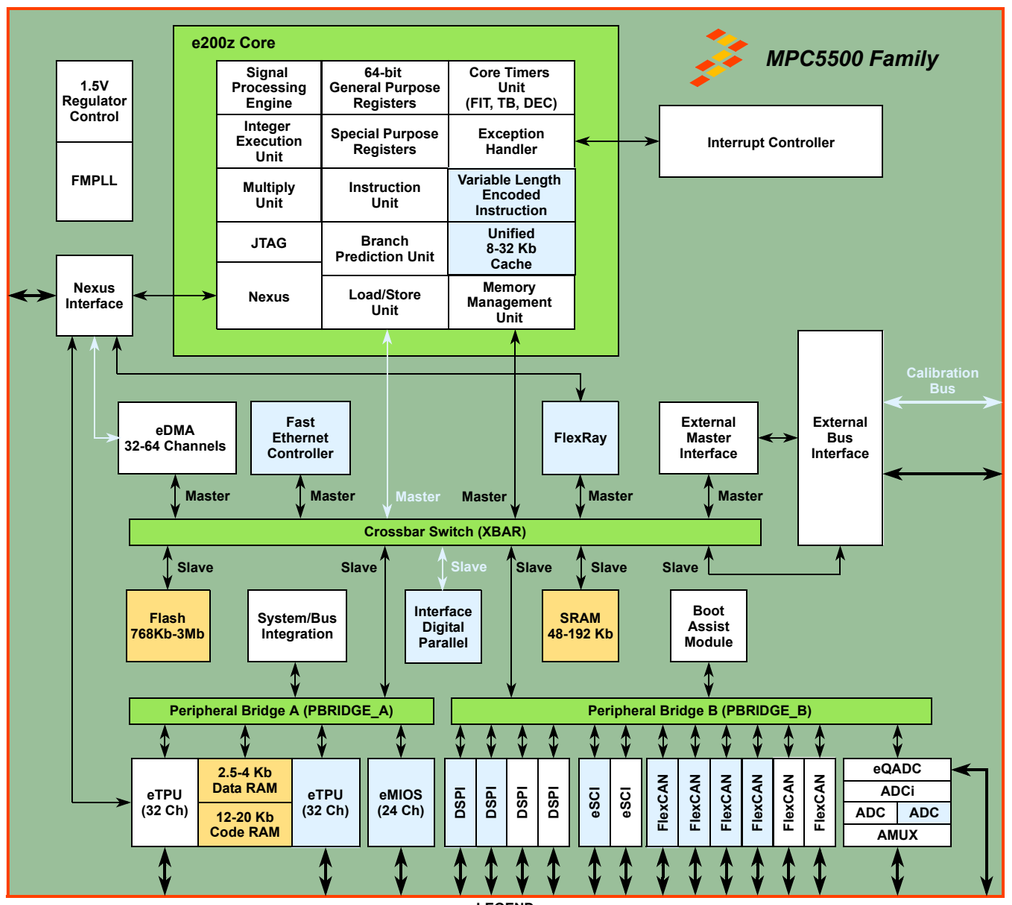
MPC5500 Family

Detailed MPC5500 Family Memory Map

Address Range[a]	Allocated Size	Used Size	Use	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
0x0000_0000–0x000B_FFFF	768 Kb	768 Kb	Flash Array	√	√	√	√	√	√	√	√
0x000C_0000–0x000F_FFFF	256 Kb	256 Kb	Flash Array		√	√	√	√	√	√	√
0x0010_0000–0x0017_FFFF	512 Kb	512 Kb	Flash Array			√	√		√	√	√
0x0018_0000–0x001F_FFFF	512 Kb	512 Kb	Flash Array				√		√	√	√
0x0020_0000–0x002F_FFFF	1 Mb	1 Mb	Flash Array							√	
0x0030_0000–0x00FF_FBFF	~13 Mb	N/A	Reserved								
0x00FF_FC00–0x00FF_FFFF	1024 bytes	1024 bytes	Flash Shadow Block	√	√	√	√	√	√	√	√
0x0100_0000–0x1FFF_FFFF	496 Mb	2 Mb	Emulation Mapping of Flash Array	√	√	√	√	√	√	√	√
0x2000_0000–0x3FFF_FFFF	512 Mb	N/A	External Memory	√	√	√	√	√	√	√	√
0x4000_0000–0x4000_7FFF	32 Kb	32 Kb	SRAM Array, Standby Powered	√	√	√	√	√	√	√	√
0x4000_8000–0x4000_BFFF	16 Kb	16 Kb	SRAM Array	√	√	√	√	√	√	√	√
0x4000_C000–0x4000_FFFF	16 Kb	16 Kb	SRAM Array		√	√	√	√	√	√	√
0x4001_0000–0x4001_3FFF	16 Kb	16 Kb	SRAM Array					√		√	√
0x4001_4000–0x4001_FFFF	48 Kb	48 Kb	SRAM Array					√		√	
0x4002_0000–0x4002_FFFF	64 Kb	64 Kb	SRAM Array					√			
0x4003_0000–0x9FFF_FFFF	(<1.5 Gb)	N/A	Reserved								
0xA000_0000–0xAFFF_FFFF	256 Mb	256 Mb	Parallel Digital Interface					√			
0xA000_0000–0xBFFF_FFFF	256 Mb	256 Mb	Reserved								
Bridge A Peripherals											
0xC000_0000–0xC3EF_FFFF	63 M	N/A	Reserved								
0xC3F0_0000–0xC3F0_3FFF	16k		Bridge A Registers	√	√	√	√	√	√	√	√
0xC3F0_4000–0xC3F7_FFFF	496 K	N/A	Reserved								
0xC3F8_0000–0xC3F8_3FFF	16 Kb		FMPLL	√	√	√	√	√	√	√	√
0xC3F8_4000–0xC3F8_7FFF	16 Kb	48	External Bus Interface (EBI) Configuration	√	√	√	√	√	√	√	√
0xC3F8_8000–0xC3F8_BFFF	16 Kb	28	Flash Configuration	√	√	√	√	√	√	√	√
0xC3F8_C000–0xC3F8_FFFF	16 Kb	N/A	Reserved								
0xC3F9_0000–0xC3F9_3FFF	16 Kb	2.5 Kb	System Integration Unit (SIU)	√	√	√	√	√	√	√	√
0xC3F9_4000–0xC3F9_FFFF	48 Kb	N/A	Reserved								
0xC3FA_0000–0xC3FA_3FFF	16 Kb	1056	Modular Timer System (eMIOS)		√	√	√	√	√	√	√
0xC3FA_4000–0xC3FA_7FFF	16 Kb	1056	Modular Timer System (eMIOS_B)[c]								
0xC3FA_8000–0xC3FB_FFFF	96 Kb	N/A	Reserved								
0xC3FC_0000–0xC3FC_3FFF	16 Kb	3 Kb	Enhanced Time Processing Unit (eTPU) Registers	√	√	√	√		√	√	√
0xC3FC_4000–0xC3FC_7FFF	16 Kb	N/A	Reserved								
0xC3FC_8000–0xC3FC_09FF	16 Kb	2.5 Kb	eTPU Shared Data Memory (Parameter RAM)	√	√	√	√		√	√	√
0xC3FC_8A00–0xC3FC_8BFF		0.5 Kb					√			√	
0xC3FC_8C00–0xC3FC_8FFF		1 Kb								√	
0xC3FC_9000–0xC3FC_BFFF			eTPU Parameter RAM Reserved								
0xC3FC_C000–0xC3FC_FFFF	16 Kb	3 Kb	eTPU Shared Data Memory (Parameter RAM) mirror	√	√	√	√		√	√	√
0xC3FD_0000–0xC3FD_2FFF	20 Kb	12 Kb	eTPU Shared Code RAM (12K,16K, or 20K)	√	√	√	√		√	√	√
0xC3FD_3000–0xC3FD_3FFF		4 Kb					√			√	
0xC3FD_4000–0xC3FD_4FFF		4 Kb								√	
0xC3FD_5000–0xC3FF_FFFF	140 Kb	N/A	Reserved								
0xC3FF_8000–0xC3FF_BFFF	16 Kb	N/A	Reserved								
0xC3FF_C000–0xC3FF_FFFF	16 Kb	N/A	Reserved								
0xC400_0000–0xDFFF_FFFF	(448 Mb)	N/A	Reserved								
Bridge B Peripherals											
0xE000_0000–0xFBFF_FFFF	(448 Mb)	N/A	Reserved								
0xFC00_0000–0xFFEF_FFFF	63 Mb	N/A	Reserved								
0xFFF0_0000–0xFFF0_3FFF	16 Kb	N/A	Bridge B Registers	√	√	√	√	√	√	√	√
0xFFF0_4000–0xFFF0_7FFF	16 Kb	N/A	Crossbar (XBAR)	√	√	√	√	√	√	√	√
0xFFF0_8000–0xFFF0_FFFF	32 Kb	N/A	Reserved								
0xFFF1_0000–0xFFF3_FFFF	192 Kb	N/A	Reserved								
0xFFF4_0000–0xFFF4_3FFF	16 Kb	N/A	ECSM	√	√	√	√	√	√	√	√
0xFFF4_4000–0xFFF4_7FFF	16 Kb	N/A	DMA Controller 2 (eDMA)	√	√	√	√	√	√	√	√
0xFFF4_8000–0xFFF4_BFFF	16 Kb	N/A	Interrupt Controller (INTC)	√	√	√	√	√	√	√	√
0xFFF4_C000–0xFFF4_C3FF	1 Kb	N/A	Fast Ethernet Controller (FEC)[b]			√				√	√
0xFFF4_C400–0xFFF4_FFFF	15 Kb	N/A	Reserved								
0xFFF5_0000–0xFFF7_FFFF	192 Kb	N/A	Reserved								
0xFFF8_0000–0xFFF8_3FFF	16 Kb	164	Enhanced Queued Analog-to-Digital Converter (eQADC)	√	√	√	√	√	√	√	√
0xFFF8_4000–0xFFF8_7FFF	16 Kb	164	Enhanced Queued Analog-to-Digital Converter (eQADC_B)[c]								
0xFFF8_8000–0xFFF8_BFFF	16 Kb	N/A	Reserved								
0xFFF8_C000–0xFFF8_FFFF	16 Kb	N/A	Reserved								
0xFFF9_0000–0xFFF9_3FFF	16 Kb	200	Deserial Serial Peripheral Interface (DSPI_A)				√			√	
0xFFF9_4000–0xFFF9_7FFF	16 Kb	200	Deserial Serial Peripheral Interface (DSPI_B)		√	√	√	√	√	√	√
0xFFF9_8000–0xFFF9_BFFF	16 Kb	200	Deserial Serial Peripheral Interface (DSPI_C)	√	√	√	√	√	√	√	√
0xFFF9_C000–0xFFF9_FFFF	16 Kb	200	Deserial Serial Peripheral Interface (DSPI_D)	√	√	√	√		√	√	√
0xFFFA_0000–0xFFFA_3FFF	16 Kb	200	Deserial Serial Peripheral Interface (DSPI_E)[c]								
0xFFFA_4000–0xFFFA_7FFF	16 Kb	200	Deserial Serial Peripheral Interface (DSPI_F)[c]								
0xFFFA_8000–0xFFFA_FFFF	32 Kb	N/A	Reserved								
0xFFFB_0000–0xFFFB_3FFF	16 Kb	44	Serial Communications Interface (SCI_A)	√	√	√	√	√	√	√	√
0xFFFB_4000–0xFFFB_7FFF	16 Kb	44	Serial Communications Interface (SCI_B)		√	√	√	√	√	√	√
0xFFFB_8000–0xFFFB_BFFF	16 Kb	44	Serial Communications Interface (SCI_C)					√			
0xFFFB_C000–0xFFFC_FFFF	16 Kb	44	Serial Communications Interface (SCI_D)					√			
0xFFFC_0000–0xFFFC_3FFF	16 Kb	1152	Controller Area Network (FlexCAN_A)	√	√	√	√	√	√	√	√
0xFFFC_4000–0xFFFC_7FFF	16 Kb	1152	Controller Area Network (FlexCAN_B)				√		√	√	√
0xFFFC_8000–0xFFFC_BFFF	16 Kb	1152	Controller Area Network (FlexCAN_C)	√	√	√	√	√	√	√	√
0xFFFC_C000–0xFFFC_FFFF	16 Kb	1152	Controller Area Network (FlexCAN_D)							√	√
0xFFFD_0000–0xFFFD_3FFF	16 Kb	1152	Controller Area Network (FlexCAN_E)								√
0xFFFD_4000–0xFFFD_FFFF	48 Kb	N/A	Reserved								
0xFFFE_0000–0xFFFE_3FFF	16 Kb	2k	FlexRay					√			√
0xFFFE_4000–0xFFFE_7FFF	16 Kb	N/A	Reserved								
0xFFFE_8000–0xFFFE_BFFF	16 Kb	32	Parallel Digital Interface					√			
0xFFFE_C000–0xFFFF_BFFF	64 Kb	N/A	Reserved								
0xFFFF_C000–0xFFFF_FFFF[d]	16 Kb	16 Kb	Boot Assist Module (BAM)	√	√	√	√	√	√	√	√
			Cache Size	**0K**	**0K**	**8K**	**32K**	**32K**	**8K**	**32K**	**8K**

a. If allocated size > used size, then the base address for the module is the lowest address of the listed address range, unless noted otherwise.
b. The Fast Ethernet controller (FEC) uses different pins on the MPC5553/MPC5566 than the MPC5567.
c. Reserved for future compatibility. No device is currently defined that uses these regions.
d. BAM address range is configured so that 4k BAM occupies 0xFFFF_F000-0xFFFF_FFFF.





LEGEND

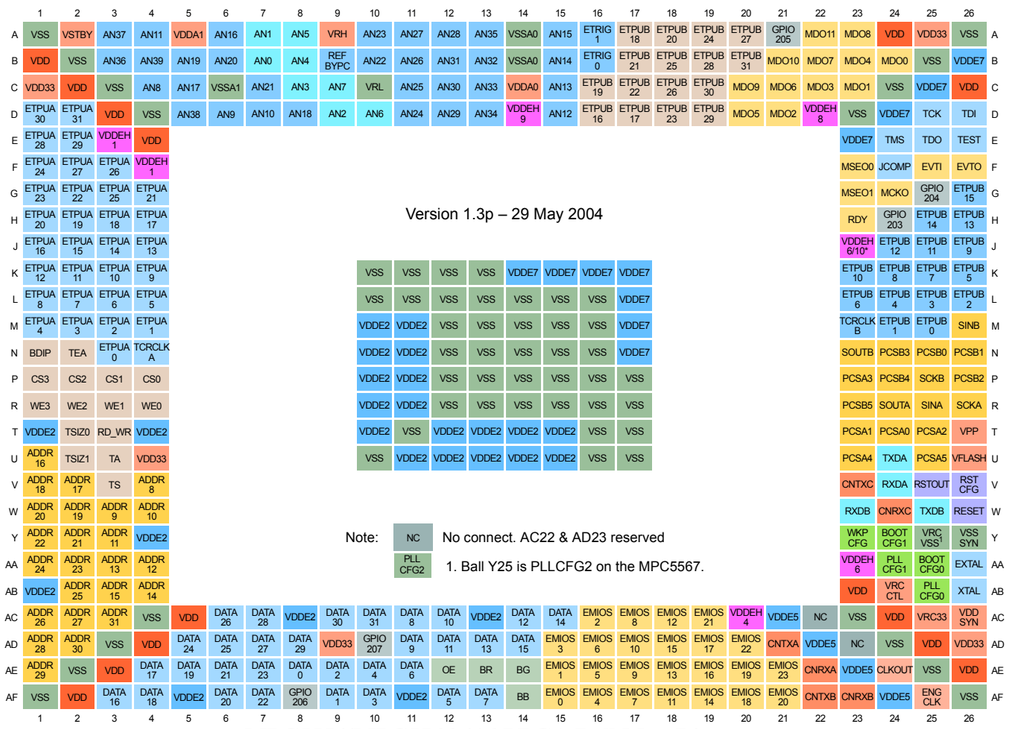
MPC5500 Device Module Acronyms

CAN – Controller area network (FlexCAN)
DSPI – Deserial/serial peripheral interface
eDMA – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued analog/digital converter
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FEC – Fast EtherNet Controller
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

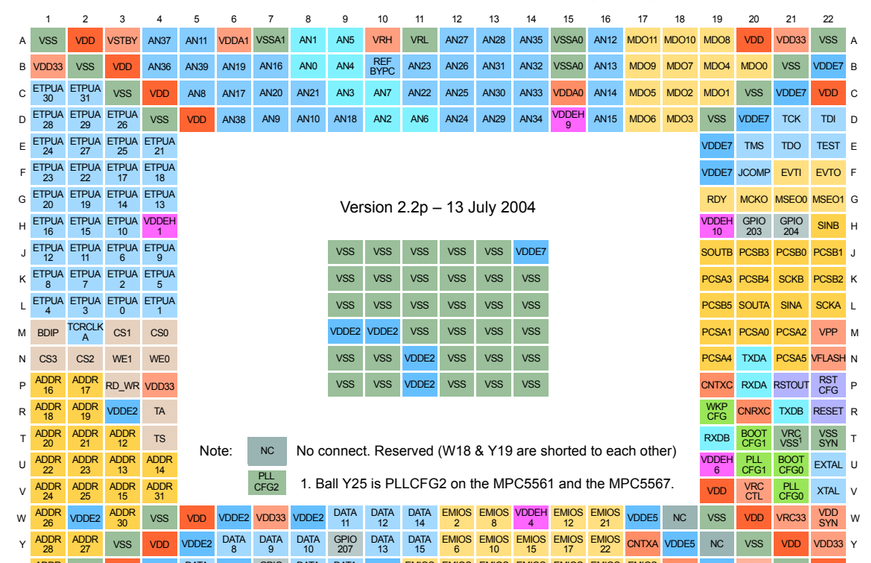
e200z Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Not available on all devices.



MPC5554/MPC5566 416 PBGA Ball Map Diagram



MPC5533/MPC5534/MPC5553/MPC5565 324 PBGA Ball Map Diagram

For more information on the MPC5500 Family, go to http://www.freescale.com/MPC55xx.